Digital Communication Systems Engineering with Software-Defined Radio

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Lecture 25

"Build It and They Will Come"

- Exploration into advanced wireless communication and networking techniques require highly flexible platforms
  - Software-defined radio very well-suited due to its rapid reconfigurable attributes
  - Allows for controlled yet realistic experimentation
- Use of real-time test bed operations enables a large set of experiments for various receiver settings, transmission scenarios, and network configurations
  - Excellent alternative for comprehensive evaluation of communication systems operating within a networked environment
  - Monte Carlo simulations can be computationally exhaustive and are only as accurate as the devised computer model

System Requirements

- Real-time baseband processing for spectrum sensing and agile transmission with high computational throughput and low latency
- Integration of physical and network layers through real-time protocol implementation on embedded processors
- Sufficiently wide bandwidth radio front-end with agility over multiple sub-channels and scalable number of antennas for spatial processing
- Central processing of information exchange between multiple radios for controlled physical and network layer development and analysis (*e.g.*, control channel implementation)

System Requirements

- Ability to perform controlled experiments in different environments (*e.g.*, shadowing and multipath, indoor and outdoor environments)
- Support for multiple radios which can be emulated as either primary users or cognitive radios
- Reconfigurability and fast prototyping through a software design flow for algorithm and protocol description

Currently Available Advanced SDR Platforms

- **Rice University WARP** – WARP radios include a Xilinx Virtex-II Pro FPGA board as well as a MAX2829 transceiver
- **Kansas University Agile Radio** – KUAR is a small form factor SDR platform containing a Xilinx Virtex-II Pro FPGA board and a PCI Express 1.4 GHz Pentium-M microprocessor
- **Lyrtech Small Form Factor SDR** – Industry collaboration between Texas Instruments and Xilinx
- **Berkeley BEE2** – BEE2 is targeted as a powerful reconfigurable computing engine with five Xilinx Virtex-II Pro FPGAs on the emulation board
- **Motorola 10 MHz-4 GHz CMOS-Based CR Platform** – Experimental wideband small form factor industrial prototype
- **Maynooth Adaptable Radio System** – Custom-built small form factor SDR platform

BEE2 Specifications

- The BWRC cognitive radio testbed hardware architecture consists of:
  - Berkeley Emulation Engine (BEE2)
  - Reconfigurable 2.4 GHz radio modems
  - Fiber link interface for connection between BEE2 and radios
- The software architecture consists of Simulink-based design flow and BEE2 specific operating system
  - Provides an integrated environment for implementation and simple data acquisition during experiments

BEE2 System Architecture

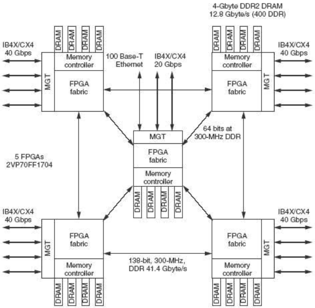

Figure : BEE2 System Architecture.

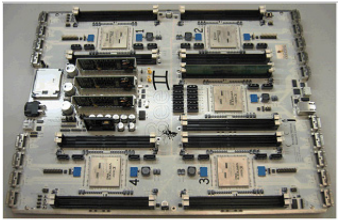

Figure : BEE2 System Implementation.

D. Cabric, D. Taubenheim, G. Cafaro, R. Farrell. "Cognitive Radio Platforms and Testbeds." in *Cognitive Radio Communications and Networks: Principles and Practice* (A. M. Wyglinski, M. Nekovee, Y. T. Hou (eds.)), Academic Press, 2009.

Reconfigurable Radio Frequency Front End

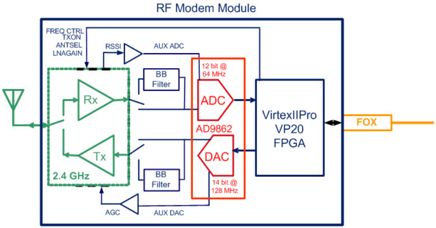

Figure : Reconfigurable 2.4 GHz Radio Modem Architecture.

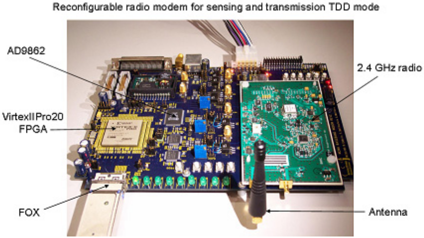

Figure : Reconfigurable 2.4 GHz Radio Modem Implementation.

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Software Design Flow

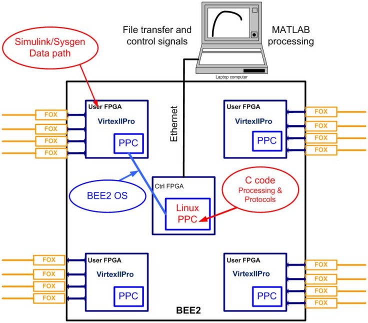

Figure : Software Design Flow for Mapping of Algorithms and Protocols on BEE2 and Experimental Control.

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Emulation Scenarios

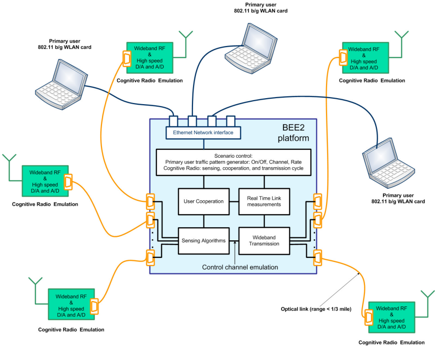

Figure : Emulation of Cognitive Radios and Primary Users.

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Case Study: Spectrum Sensing

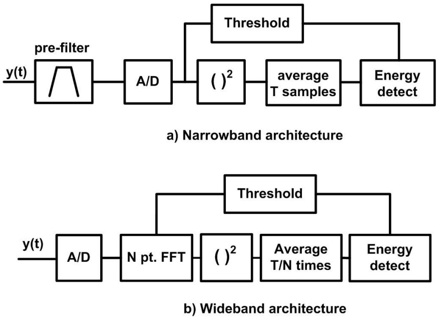

Figure : Energy Detector Implementations: a) Narrowband Architecture, b) Wideband Architecture.

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Case Study: Spectrum Sensing

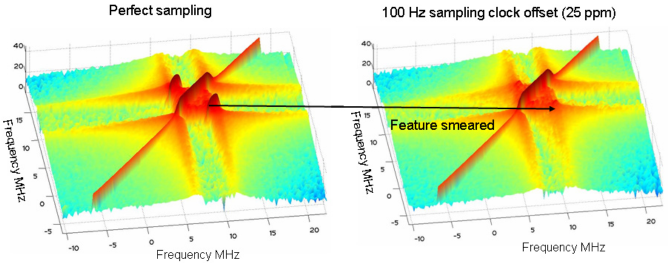

Figure : Spectral Correlation Function of 4MHz QPSK Signal with Perfect Sampling (left) and with 100Hz Sampling Offset (right).

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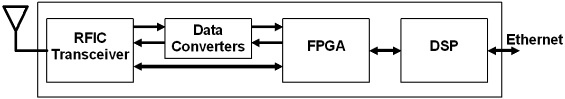
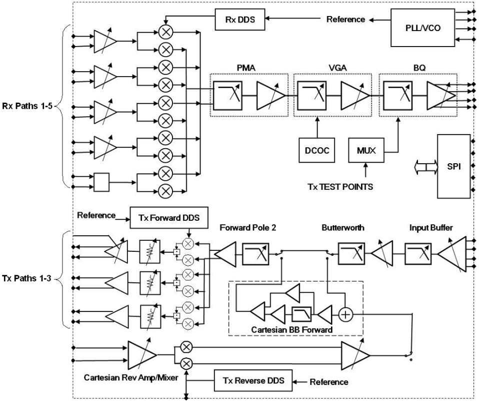
Platform Specifications

- Fundamentally flexible, low-power transceiver integrated circuit (IC) at the core of this experimental platform
  - Enables realization of a small form-factor, experimental cognitive radio (CR) devices
- Through flexible programming of this “RFIC” (radio frequency IC), the platform can receive and transmit signals of many wireless protocols–standard or experimental
  - Carrier frequencies from 10 MHz to 4 GHz with channel bandwidths from 8 kHz to 20 MHz supported



RFIC Architecture



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Device Form Factor

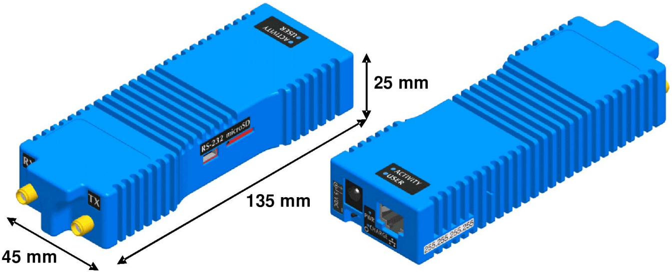

Figure : Exterior View of CR Platform.

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System Component Integration

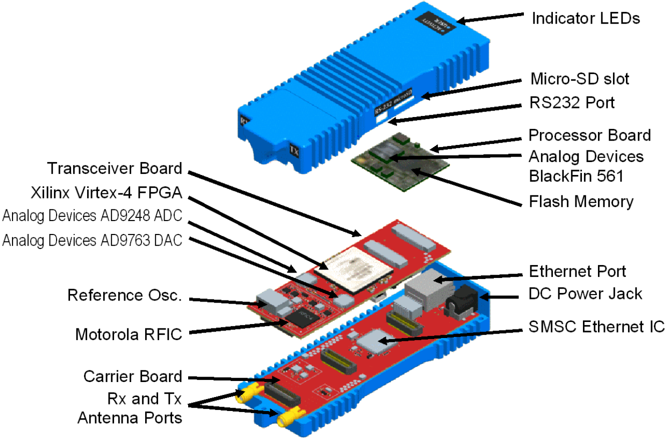

Figure : Exploded View of CR Platform and its Components.

Platform Logical Structure

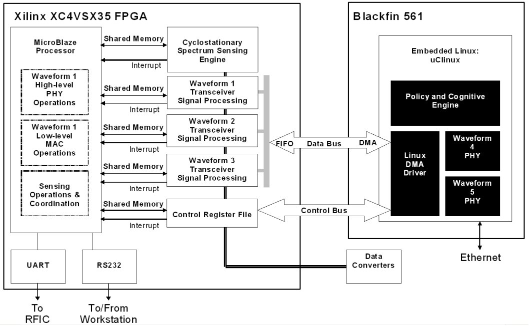

Figure : Logical Structure of the CR Platform.

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Case Study: Cyclostationary Analysis

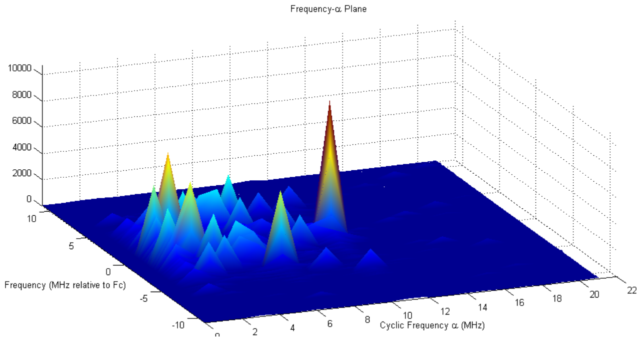

Figure : MATLAB Plot of On-channel f-α Plane Calculated by CSS Block in FPGA.

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MARS Specifications

- MARS platform had the original objectives of being a personal computer connected radio front-end where all the signal processing is implemented on the computers general purpose processor
- MARS platform designed to deliver performance equivalent to that of a future basestation and the wireless communication standards in 1700 MHz to 2450 MHz frequency range
  - Communication standards GSM1800, PCS1900, IEEE 802.11b/g, UMTS (TDD and FDD) are supported
  - Full-band support should be explored, 70 MHz over an approximate 700 MHz range for future wireless applications and services

MARS System Overview

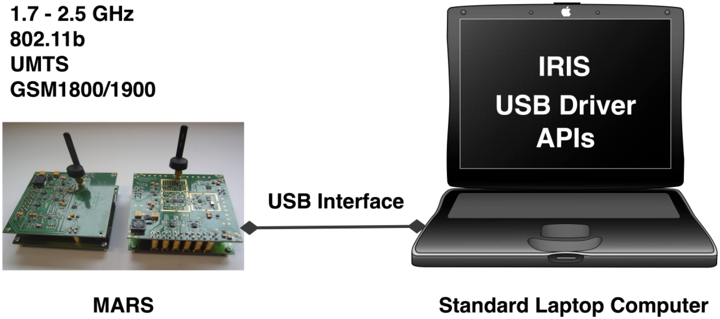

Figure : Maynooth Adaptable Radio System (MARS) Platform.

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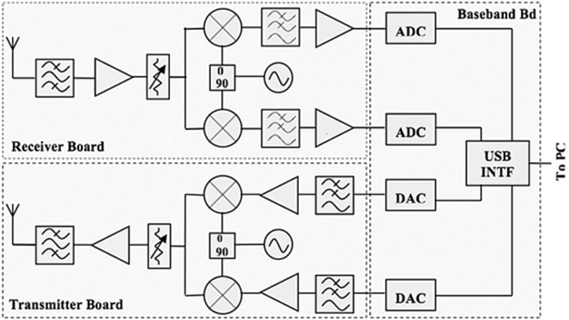
MARS Architecture



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Software Radio Engine

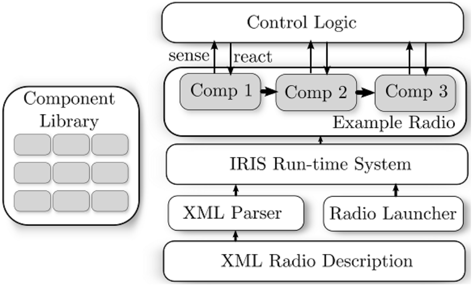

Figure : IRIS Software Radio Architecture.

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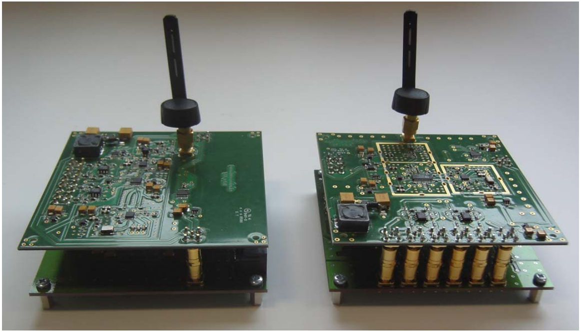
Modular MARS Transmitter and Receiver Platforms



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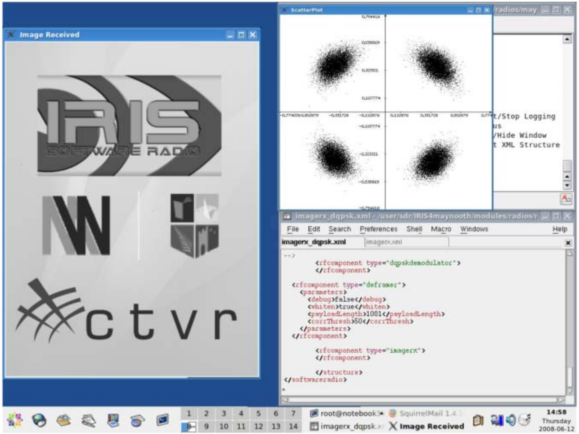
Case Study: QPSK Transmission



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