Logic Gate Design

3 inputs and 2 output systems.

In class, we have seen two input one output system. We will design a bigger system in this assignment using three inputs A, B and C that effect two outputs, P and Q. Please note that outputs P and Q are not related to each other. They can be related but let us assume they are not related at this point.

Let us assume the system outputs depend on the inputs in following way.

A	B	C		P	Q
0	0	0		0	1
0	0	1		0	1
0	1	0		1	0
0	1	1		0	1
1	0	0		1	0
1	0	1		1	0
1	1	0		1	1
1	1	1		0	0

We will do the design for output P and design for output Q will be left as an assignment.

Design for Output P

Clearly, as it is a 3 input system, number of states is $2^n = 2^3 = 8$.

Let us number these states starting from 0 to 7,

State Number	A	B	C		P	Q
0	0	0	0		0	1
1	0	0	1		0	1
2	0	1	0		1	0
3	0	1	1		0	1
4	1	0	0		1	0
5	1	0	1		1	0
6	1	1	0		1	1
7	1	1	1		0	0

Now, let us make a map for these states where we can give address to each of the state in terms of inputs A, B and C.

	A'	**A'**	**A**	**A**
C'	000 State 0	010 State 2	110 State 6	100 State 4
C	001 State 1	011 State 3	111 State 7	101 State 5
	B'	**B**	**B**	**B'**

Now, let us start with designing logic gate circuit for output P.

We will mark all the states in the map wherever we see the output (wherever P = 1)

P	**A'**	**A'**	**A**	**A**
C'	000 State 0	010 1 State 2	110 1 State 6	100 1 State 4
C	001 State 1	011 State 3	111 State 7	101 1 State 5
	B'	**B**	**B**	**B'**

Now we put addresses of states wherever we see output for P.

P is present (value 1) at State 2 or 4 or 5 or 6.

Adress of each state where P is present:

State	Address
2	A'.B.C' (A NOT there and B there and C NOT there)
4	A.B'.C' (A there and B NOT there and C NOT there)
5	A.B'.C (A there and B NOT there and C there)
6	A.B.C' (A there and B there and C NOT there)

Hence, P = A'.B.C' + A.B'.C' + A.B'.C + A.B.C'

Question 1: Can you design gate design for this? Draw in the space provided below. (10 Points)

Answer:

Question 2: How many gates will you need? (5 Points)

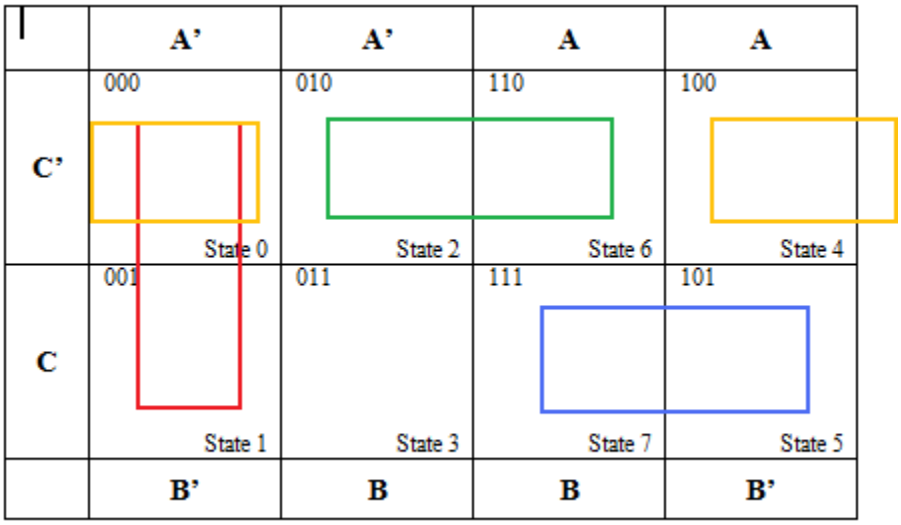
Answer:

Question 3: Design the circuit for the output Q. How many gates do you need? (30 Points)

More efficient circuits

Is the solutions for P and Q we just achieved optimum? Can we have a design which uses lesser gates? Reducing number of gates results in less cost, and less complex design.

Let us try out. Before that, let us take a step back and think. If you buy two plots of land, how will you address the combined thing?



This figure above shows some pair of states combined together. I have bought states 2 and 6 and want to address it. How can I do that? Let us see…

My plot (In green) is not on C, it is on C'. Also, it is on B and not on B'. It covers both A and A'. So giving address in terms of A won't make sense. We will give address in terms of B and C only. And here is how we do it.

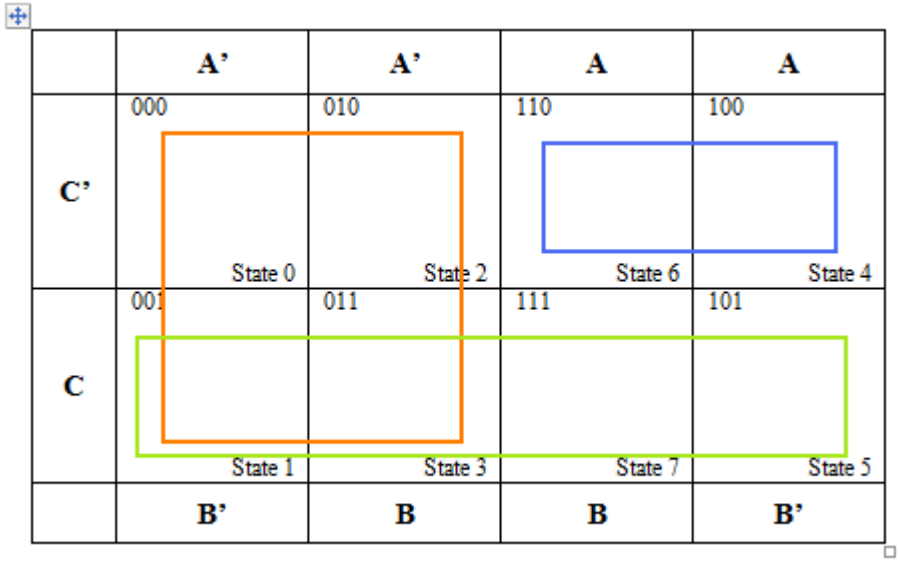
Address of Green plot = B.C'

Now, note that if you move from state 4 to the right, you enter state 0. If you move from state 4 to the top, you enter state 5. This works for all the states that lie on the edge of the map. It is like "Snakes" without any wall!

So, we can say that we can buy state 4 and state 0, group it together to form one plot of land. How do we address it? We again follow the same logic of finding presence of A, B and C. C is not present, C' is present. B is not present, B' is present. Again, A is present in one and not present in other state. So we do not write A in the address as it would be meaningless to do so in writing the address of the plot.

Hence, the address of the Yellow plot is B'.C'.

Question 4: Can you give address of following plots? (15 Points)



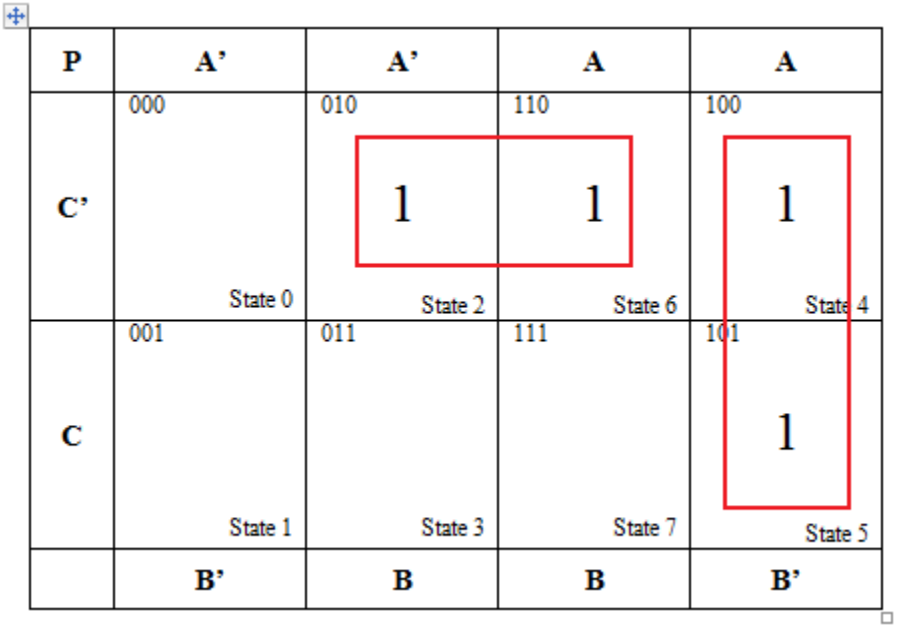
Answer:

Red:

Blue:

Green:

Now, let us go back again to find optimum design for output P in our initial problem.



We can club the 4 states into pairs of 2 or 4 (or 8 or 16 or so on… in higher order cases) and we can do that in many numbers of ways. So there is no fixed way of doing so. Let us do it in a way as shown above (marked in Red).

Here, Combining state 2 and 6 we get one plot. And combining state 4 and 5, we get another plot.

Now, P, the output is present either in plot 1 or in plot 2.

Question 5: Can you give the simplified address of P now? Write it in the space provided. (5 points)

Answer:

Question 6: Can you draw the circuit diagram for this address? Draw it in the space provided. (15 points)

Answer:

Question 7: Design a better circuit for the output Q than what you have already drawn. How many gates do you need? (20 points)

Extra Credit (50 Points)

4 Input 2 Output System

Following is the state chart (truth table) of a 4-input 2-output system. Design a logic diagram using logic gates to implement logic for M (25 points) and N (25 points).

Inputs					Outputs	
A	**B**	**C**	**D**		**M**	**N**
0	0	0	0		0	1
0	0	0	1		0	1
0	0	1	0		0	1
0	0	1	1		1	1
0	1	0	0		1	0
0	1	0	1		1	0
0	1	1	0		1	0
0	1	1	1		0	1
1	0	0	0		0	1
1	0	0	1		0	1
1	0	1	0		1	1
1	0	1	1		1	0
1	1	0	0		1	0
1	1	0	1		1	0
1	1	1	0		0	1
1	1	1	1		0	1

Hint: State map for 4-input system looks something like this. States are not marked but they are 16 in number. Mark the states with their addresses as the first step.

	A'	**A'**	**A**	**A**	
C'					**D'**
C'					**D**
C					**D**
C					**D'**
	B'	**B**	**B**	**B'**	