Instruction Timing

(See Notes)

Appendix B of Cortex A-9 Technical Reference Manual

the wait() function from lab #3

– time delay

the op codes (instruction) used

ldr, str	- 2	clock cycles	load/store register
add, sub	- 1	clock cycles	
cmp, nop	- 1	clock cycles	compare no operation
bne	- 0	clock cycles	branch if not equal
push ldmfd	- 2	clock cycles	Stack operations

I suggest that you copy the assembly language from the assignment to a spreadsheet to compute the total number of cycles ⇒ execution time

the clock frequency is 667 MHz