Laboratory 1:
Dissection of Electronic Packaging

ME/MSE 487 AA/AB Autumn 2007
Electronic Packaging Laboratory

Objective

To gain an understanding of the structure and function of the components in first level electronic packages.

Introduction

Electronic packaging can be referred to as the housing and interconnection of integrated circuits (ie: chips, die) to form an electronic system. The package must provide adequate heat dissipation, power distribution, circuit support, and circuit protection. In addition, an electronic package must maintain high performance levels while still allowing for a product that is high quality, reliable, serviceable, and economical [1].

Typical electronic packages consist of a hierarchy of interconnections that can be divided up into levels ranging from 0 to 6. The main focus for this laboratory is the first level package; named the first level because it contains only a single die. A cross section of the basic first level package showing structure and components is shown below in Figure 1.

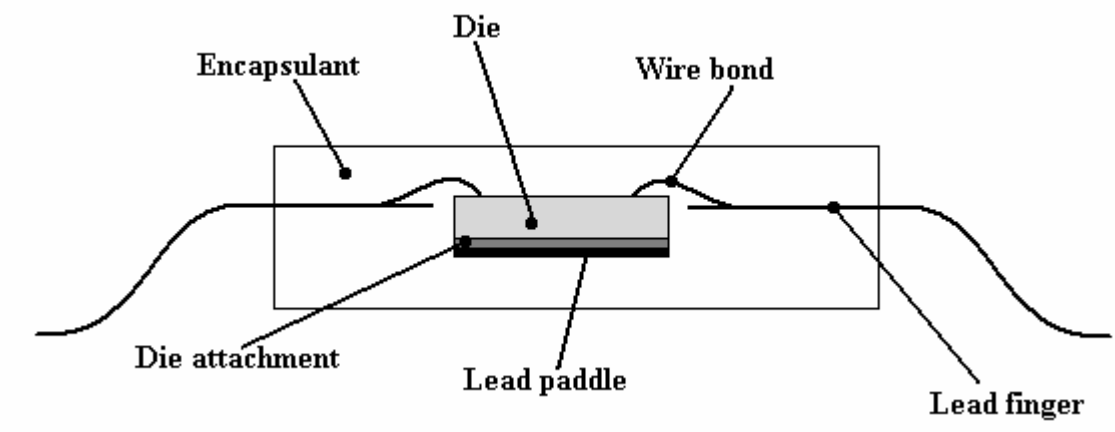

Figure 1: Cross-section of a typical first level package.

As shown in Figure 1, the first level package consists of the following 5 main components: lead frame, die, die attach, wire bond, and encapsulant. The lead frame includes both the lead paddle and lead finger. The lead paddle is used to mechanically support the die before encapsulation while the lead finger allows for electrical contact between the package and circuit board. The die attach material permits heat conduction

while assuring mechanical stability of the die. Wire bonding is used to electrically connect the die to the lead fingers. This technique involves connecting aluminum or gold wires between the die bonding pads and the contact points on the package. Finally, the encapsulant is used to protect the die and also gives support to the components within the package. The encapsulant material is either a polymer or ceramic, depending on cost and the environment in which the package is used [1].

The package family selected for an electronic application is dependent on the chip power, size and weight requirements of the system, electrical performance, and lead count requirements. First level packages can be classified into four main groups: In-Line, Small Outline, Quad Surface Mount, and Grid Array. This grouping is based on lead count (number of leads on a package) and lead position. Table 1 contains examples of the four main groups and gives examples of each group.

Table 1: Package Families [2]

Package Family	**Characteristics**	**Package Type**
In-Line	Leads on one or two sides of package	SIP, PDIP, CERDIP
Small Outline	Leads on two or four sides, small body	SOJ, SOP, TSOP
Quad Surface Mount	Leads on four sides of package Larger package dimension High lead counts	PLCC, PQFP, LDCC, CERQUAD
Grid Array	Pin or ball array placed on package body Very high lead count.	PPGA, PLGA, PBGA

- The In-Line package family contains SIP, PDIP, and CERDIP. SIP, or single in-line package, has leads located only on one side of the package. Since the leads are located on just one side, these memory chips can be placed side by side, separated only by the thickness of the package.

- Small Outline Family contains SOJ, SOP, and TSOP. SOP, or small outline gull-wing package, has leads on two sides of the package. This package is usually for small die sizes and is commonly used for SRAM chips. The SOP Package is shown below in Figure 2.

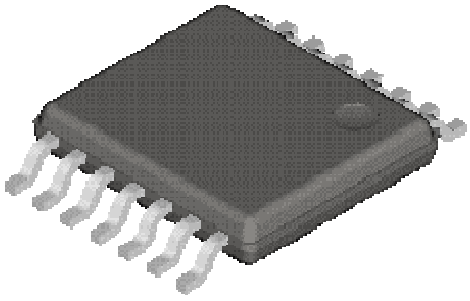

Figure 2: Small outline gull-wing package (SOP)

- The Quad Surface Mount Family is comprised of packages with lager bodies and higher lead counts. The PQFP which stands for Plastic Quad Flat Package is shown in Figure 3. The PQFP has a large body and high lead counts with leads placed on all four sides of the package. This is a very versatile and scalable package whose lead counts can be modified depending on the needs of the chip and package. The Quad Surface Mount family also includes the PLCC (Plastic Leaded Chip Carrier) as shown in Figure 3.

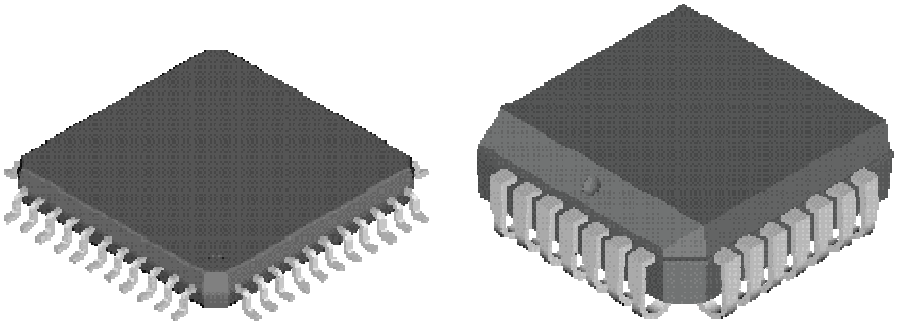

Figure 3: PQFP (Plastic Quad Flat Pack) & PLCC (Plastic Leaded Chip Carrier)

- The Grid Array family is comprised of packages that have a rectangular pin or ball array on the package body. These packages are high-density, high-performance and typically contain large numbers of leads. An Example of this family is the PPGA (Plastic Pin Grid Array) shown in Figure 4.

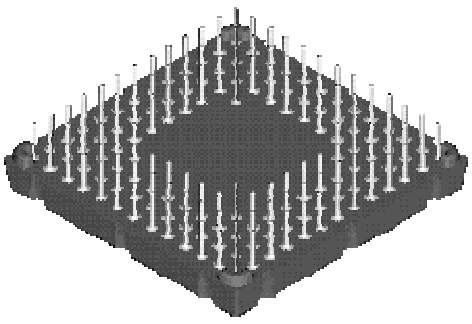

Figure 5: PPGA (Plastic Pin Grid Array)

Experimental Equipment

- SOP, PLCC, and/or PLGA Packages
- Grinder/Abrasive Papers
- Optical Microscope
- Floppy Disk
- Calipers

Procedure

1. Break into small groups of four people.
2. Each group will be assigned a particular package type (SOP, PLCC, or PLGA) for dissection. Also, each person within the group will be assigned a specific view to examine: wire bonds, die pattern, lead frame, or cross-section.
3. The groups will carefully grind and polish the assigned package using the MSE polishing and microscopy laboratories (Meuller Hall/MEB) to show the wire bonds, die pattern, lead frame, and cross-section of the assigned package. Show each of these views on a separate specimen. *Note: In order to produce a good quality specimen, this process must be completed slowly and methodically. So, relax and be patient!*
4. Examine specimens with the optical microscope and take pictures if necessary.
5. Each group member will use the calipers to measure the dimensions of their specimen and will then discuss the findings with their group.
6. *Report Findings Individually*

Items to be included in discussion:

1. Discuss the purpose of packaging and the application of your assigned packages.
2. Describe and sketch the top view, side view, and cross-sectional view of both assigned packages with dimensions. Include aspects like package length, width, height, pin spacing, footprint width, lead count, etc…
3. Construct a 3-D model of the inside of both the assigned packages and discuss the function of each component. Do not include dimensions. *Note: The 3-D models can be drawn by hand (sketch) or using a computer program (ie: MS paint). It is to show the locations of package components in the absence of the encapsulant. Focus on the science rather than the artwork.*
4. From the viewpoint of a material scientist, discuss the design requirements of the following components: lead frame, die attach, wire bonding wire, and encapsulant.

Questions

1. Explain the hierarchy of packaging with drawings. (levels 0-6)
2. Define and show sketches of the following terms:

BGA	CERDIP	PGA	SOJ
C4	LDCC	PDIP	SOP
CERQUAD	CLCC	PPGA	

Note: answer left to right and top to bottom

3. Define the following terms:

LGA	MCR	PWB	TCP
CPGA	MQFP	SBA	TQFP
ILB	MQUAD	SIMM	TSOP
EQFP	OLB	SIP	VFQFP
FQFP	PCB	SOIC	ZIP
TAB			

Note: answer left to right and top to bottom

References

1. W.D. Brown (ed.). Advanced Electronic Packaging. New York, IEEE Press, 1999.

2. R.J. Hannemann, A.D. Kraus, and Michael Pecht. Physical Architecture of VLSI Systems. New York, John Wiley & Sons, Inc., 1994.

3. D.P. Seraphim, R. Lasky, and C. Li. Principles of Electronic Packaging. New York, Mcgraw-Hill, 1989.