Low-Power, High-Speed CMOS Analog Switches

**Features**
- 44-V Supply Max Rating
- ±15-V Analog Signal Range
- On-Resistance—$r_{DS(on)}$: 20 Ω
- Low Leakage—$I_{D(on)}$: 40 pA
- Fast Switching—$t_{ON}$: 100 ns
- Ultra Low Power
  - Requirements—$P_D$: 0.35 μW
- TTL, CMOS Compatible
- Single Supply Capability

**Benefits**
- Wide Dynamic Range
- Low Signal Errors and Distortion
- Break-Before-Make Switching Action
- Simple Interfacing

**Applications**
- Audio and Video Switching
- Sample-and-Hold Circuits
- Battery Operation
- Test Equipment
- Hi-Rel Systems
- PBX, PABX

**Description**

The DG401/403/405 monolithic analog switches were designed to provide precision, high performance switching of analog signals. Combining low power (0.35 μW, typ) with high speed ($t_{ON}$: 100 ns, typ), the DG401 series is ideally suited for portable and battery powered industrial and military applications.

Built on the Siliconix proprietary high-voltage silicon-gate process to achieve high voltage rating and superior switch on/off performance, break-before-make is guaranteed for the SPDT configurations. An epitaxial layer prevents latchup.

Each switch conducts equally well in both directions when on, and blocks up to 30 V peak-to-peak when off. On-resistance is very flat over the full ±15-V analog range, rivaling JFET performance without the inherent dynamic range limitations.

The three devices in this series are differentiated by the type of switch action as shown in the functional block diagrams.

**Functional Block Diagrams and Pin Configurations**

![Functional Block Diagrams](image)

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70049.
Two SPDT Switches per Package

Truth Table

<table>
<thead>
<tr>
<th>Logic</th>
<th>SW₁, SW₂</th>
</tr>
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<tbody>
<tr>
<td>0</td>
<td>OFF</td>
</tr>
<tr>
<td>1</td>
<td>ON</td>
</tr>
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Logic “0” ≤ 0.8 V
Logic “1” ≥ 2.4 V

Two DPST Switches per Package

Truth Table

<table>
<thead>
<tr>
<th>Logic</th>
<th>Switch</th>
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<tr>
<td>0</td>
<td>OFF</td>
</tr>
<tr>
<td>1</td>
<td>ON</td>
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</table>

Logic “0” ≤ 0.8 V
Logic “1” ≥ 2.4 V
Ordering Information

<table>
<thead>
<tr>
<th>Temp Range</th>
<th>Package Type</th>
<th>Part Number</th>
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<tbody>
<tr>
<td>DG401</td>
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<td></td>
</tr>
<tr>
<td>–40 to 85°C</td>
<td>16-Pin Plastic DIP</td>
<td>DG401DJ</td>
</tr>
<tr>
<td>–55 to 125°C</td>
<td>16-Pin Ceramic DIP</td>
<td>DG401AK/883</td>
</tr>
<tr>
<td></td>
<td>LCC-20</td>
<td>5962-896301M2A</td>
</tr>
<tr>
<td>DG403</td>
<td></td>
<td></td>
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<tr>
<td>–40 to 85°C</td>
<td>16-Pin Plastic DIP</td>
<td>DG403DJ</td>
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<tr>
<td>–55 to 125°C</td>
<td>16-Pin Ceramic DIP</td>
<td>DG403AK/883</td>
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<td></td>
<td>LCC-20</td>
<td>5962-896301I2A</td>
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<tr>
<td>DG405</td>
<td></td>
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<tr>
<td>–40 to 85°C</td>
<td>16-Pin Plastic DIP</td>
<td>DG405DJ</td>
</tr>
<tr>
<td>–55 to 125°C</td>
<td>16-Pin Ceramic DIP</td>
<td>DG405AK/883</td>
</tr>
</tbody>
</table>

Absolute Maximum Ratings

V+ to V–: 44 V
GND to V–: 25 V
V_L: (GND – 0.3 V) to (V+) +0.3 V
Digital Inputs: V_S, V_D: (V–) –2 V to (V+ plus 2 V) or 30 mA, whichever occurs first
Current (Any Terminal) Continuous: 30 mA
Current, S or D (Pulsed 1 ms 10% duty): 100 mA
Storage Temperature: (AK, AZ Suffix) −65 to 150°C
(DJ, DY Suffix) −65 to 125°C

Power Dissipation (Package): b
16-Pin Plastic DIP: 450 mW
16-Pin Ceramic DIP: 900 mW
16-Pin SOIC: 600 mW
LCC-20: 900 mW

Notes:

a. Signals on S_X, D_X, or IN_X exceeding V+ or V– will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC Board.
c. Derate 6 mW/°C above 75°C
d. Derate 12 mW/°C above 75°C
e. Derate 7.6 mW/°C above 75°C
f. Derate 13 mW/°C above 75°C
## Specifications\textsuperscript{a}

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions Unless Specified</th>
<th>Temp\textsuperscript{b}</th>
<th>A Suffix −55 to 125°C</th>
<th>D Suffix −40 to 85°C</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Signal Range\textsuperscript{c}</td>
<td>$V_{\text{ANALOG}}$</td>
<td></td>
<td>Full</td>
<td>−15</td>
<td>15</td>
<td>−15</td>
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<tr>
<td>Drain-Source On-Resistance</td>
<td>$r_{DS(on)}$</td>
<td>$I_S = -10 , \text{mA}, V_D = \pm 10 , \text{V}$</td>
<td>Room</td>
<td>20</td>
<td>35</td>
<td>45</td>
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<tr>
<td>Δ Drain-Source On-Resistance</td>
<td>$\Delta r_{DS(on)}$</td>
<td>$I_S = -10 , \text{mA}, V_D = \pm 5 , \text{V}, 0 , \text{V}$</td>
<td>Room</td>
<td>3</td>
<td>3</td>
<td>5</td>
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<tr>
<td>Switch Off Leakage Current</td>
<td>$I_{S(\text{off})}$</td>
<td>$V_+ = 16.5, V_- = -16.5 , \text{V}$</td>
<td>Room, Hot</td>
<td>−0.01</td>
<td>−0.25</td>
<td>0.25</td>
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<tr>
<td>Channel On Leakage Current</td>
<td>$I_{D(\text{on})}$</td>
<td>$V_+ = 16.5, V_- = -16.5 , \text{V}$</td>
<td>Room, Hot</td>
<td>−0.04</td>
<td>−0.4</td>
<td>0.4</td>
</tr>
<tr>
<td>Digital Control</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current $V_{\text{IN Low}}$</td>
<td>$I_{IL}$</td>
<td>$V_{\text{IN}}$ under test = 0.8 , \text{V}$</td>
<td>Full</td>
<td>0.005</td>
<td>−1</td>
<td>1</td>
</tr>
<tr>
<td>Input Current $V_{\text{IN High}}$</td>
<td>$I_{IH}$</td>
<td>$V_{\text{IN}}$ under test = 2.4 , \text{V}$</td>
<td>Full</td>
<td>0.005</td>
<td>−1</td>
<td>1</td>
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<tr>
<td>Dynamic Characteristics</td>
<td></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Turn-On Time</td>
<td>$t_{ON}$</td>
<td></td>
<td>Room</td>
<td>100</td>
<td>150</td>
<td>150</td>
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<tr>
<td>Turn-Off Time</td>
<td>$t_{OFF}$</td>
<td></td>
<td>Room</td>
<td>60</td>
<td>100</td>
<td>100</td>
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<tr>
<td>Break-Before-Make Time Delay (DG403)</td>
<td>$t_D$</td>
<td>$R_L = 300 , \Omega, C_L = 35 , \text{pF}$</td>
<td>Room</td>
<td>12</td>
<td>5</td>
<td>5</td>
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<tr>
<td>Charge Injection</td>
<td>$Q$</td>
<td>$C_L = 10,000 , \text{pF}$</td>
<td>Room</td>
<td>60</td>
<td>50</td>
<td>50</td>
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<tr>
<td>Off Isolation Reject Ratio</td>
<td>$OIRR$</td>
<td></td>
<td>Room</td>
<td>72</td>
<td></td>
<td></td>
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<tr>
<td>Channel-to-Channel Crosstalk</td>
<td>$X_{\text{TALK}}$</td>
<td></td>
<td>Room</td>
<td>90</td>
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<tr>
<td>Source Off Capacitance</td>
<td>$C_S(\text{off})$</td>
<td></td>
<td>Room</td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Drain Off Capacitance</td>
<td>$C_D(\text{off})$</td>
<td></td>
<td>Room</td>
<td>12</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Channel On Capacitance</td>
<td>$C_{D, C_S(\text{on})}$</td>
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<td>Room</td>
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<tr>
<td>Power Supplies</td>
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<td></td>
</tr>
<tr>
<td>Positive Supply Current</td>
<td>$I_+$</td>
<td>$V_+ = 16.5 , \text{V}, V_- = -16.5 , \text{V}$</td>
<td>Room, Full</td>
<td>0.01</td>
<td>1</td>
<td>5</td>
</tr>
<tr>
<td>Negative Supply Current</td>
<td>$I_-$</td>
<td>$V_+ = 16.5 , \text{V}, V_- = -16.5 , \text{V}$</td>
<td>Room, Full</td>
<td>−0.01</td>
<td>−1</td>
<td>−5</td>
</tr>
<tr>
<td>Logic Supply Current</td>
<td>$I_L$</td>
<td>$V_{\text{IN}} = 0$ or 5 , \text{V}$</td>
<td>Room, Full</td>
<td>0.01</td>
<td>1</td>
<td>5</td>
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<tr>
<td>Ground Current</td>
<td>$I_{\text{GND}}$</td>
<td></td>
<td>Room, Full</td>
<td>−0.01</td>
<td>−1</td>
<td>−5</td>
</tr>
</tbody>
</table>

Notes:
\textsuperscript{a} Refer to PROCESS OPTION FLOWCHART.
\textsuperscript{b} Room = 25°C, Full = as determined by the operating temperature suffix.
\textsuperscript{c} Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
\textsuperscript{d} The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
\textsuperscript{e} Guaranteed by design, not subject to production test.
\textsuperscript{f} $V_{\text{IN}}$ = input voltage to perform proper function.

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S-53748—Rev. E, 05-Jun-97
Typical Characteristics

Input Switching Threshold vs. Logic Supply Voltage

V+ = 15 V, V– = –15 V
T_A = 25°C

Input Switching Threshold vs. Supply Voltages

V_L = 7 V
V_L = 5 V

r_DS(on) vs. V_D and Temperature

V+ = 15 V, V– = –15 V
V_L = 5 V

r_DS(on) vs. V_D and Power Supply Voltage

T_A = 25°C
± 6 V
± 10 V
± 12 V
± 15 V
± 20 V
± 22 V

r_DS(on) vs. V_D and Power Supply Voltage

T_A = 25°C

Charge Injection vs. Analog Voltage

V+ = 15 V, V– = –15 V
V_L = 5 V

Charge Injection vs. Analog Voltage

C_L = 10 k pF
1 k pF
100 pF

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S-53748—Rev. E, 05-Jun-97
Typical Characteristics (Cont’d)

Leakage Current vs. Temperature

Leakage Current vs. Analog Voltage

Supply Current vs. Temperature

Switching Time vs. Temperature*

Supply Current vs. Power Supply Voltage*

Switching Time vs. Positive Supply Voltage*

<table>
<thead>
<tr>
<th>V+, V– Positive and Negative Supplies (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>V+ = 15 V, V– = –15 V</td>
</tr>
<tr>
<td>V+ = 15 V, V– = –15 V</td>
</tr>
</tbody>
</table>

*I Refer to Figure 2 for test conditions.
Schematic Diagram (Typical Channel)

Figure 1.

Test Circuits

$V_O$ is the steady state output with the switch on. Feedthrough via switch capacitance may result in spikes at the leading and trailing edge of the output waveform.

$C_L$ (includes fixture and stray capacitance)

$V_O = V_S \frac{R_L}{R_L + r_{DS(on)}}$

* $V_S = 10\text{V}$ for $t_{ON}$, $V_S = -10\text{V}$ for $t_{OFF}$

Note: Logic input waveform is inverted for switches that have the opposite logic sense control

Figure 2. Switching Time

Figure 3. Break-Before-Make
Test Circuits (Cont’d)

Figure 4. Charge Injection

Off Isolation = 20 log $\frac{V_S}{V_O}$

C = RF bypass

Figure 5. Off Isolation

Insertion Loss

Figure 6.

Crosstalk

$x_{\text{TALK}}$ Isolation = 20 log $\frac{V_S}{V_O}$

C = RF bypass

Figure 7. Crosstalk

Capacitances

Figure 8.
Applications

Stereo Source Selector:

A single logic signal controls the status of all four switches of the device, simplifying stereo source switching. The low on-resistance (<35 Ω) minimizes total harmonic distortion.

Dual Slope Integrators:

The DG403 is well suited to configure a selectable slope integrator. One control signal selects the timing capacitor \( C_1 \) or \( C_2 \). Another one selects \( e_{in} \) or discharges the capacitor in preparation for the next integration cycle.

Band-Pass Switched Capacitor Filter:

Single-pole double-throw switches are a common element for switched capacitor networks and filters. The fast switching times and low leakage of the DG403 allow for higher clock rates and consequently higher filter operating frequencies.

Figure 9. Stereo Source Selector

Figure 10. Dual Slope Integrator

Figure 11. Band-Pass Switched Capacitor Filter
Applications (Cont’d)

Peak Detector:

$A_3$ acting as a comparator provides the logic drive for operating $SW_1$. The output of $A_2$ is fed back to $A_3$ and compared to the analog input $e_{in}$. If $e_{in} > e_{out}$ the output of $A_3$ is high keeping $SW_1$ closed. This allows $C_1$ to charge up to the analog input voltage. When $e_{in}$ goes below $e_{out}$ $A_3$ goes negative, turning $SW_1$ off. The system will therefore store the most positive analog input experienced.

![Figure 12. Positive Peak Detector](image-url)