Physics 334, Winter Quarter 2011, Examination #2

Name _____

1	/30
2	/25
3	/20
4	/25
TOTAL	/100

Exam notes: The exam is closed-book. You may use a calculator. You may not use your own equation sheet. Please check that you have a total of 6 pages, including this page. You may make reasonable assumptions based on standard component tolerances of 5%, which may save you some time. You may use scratch paper or the back pages of the exam, but it won't be graded.

Possibly useful equations and information:

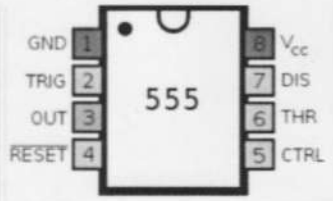
Ideal op-amp golden rules: (1) inputs source or sink no current; (2) open-loop output voltage is $(V^+ - V^-)$ times an arbitrarily large gain; (3) if properly negatively fed-back, the inputs are at the same voltage.

Tranconductance of a FET is the change in the drain current for a change in the gate-to-source voltage.

The "3 dB" frequency of an RC high- or low-pass filter is $1/(2\pi RC)$

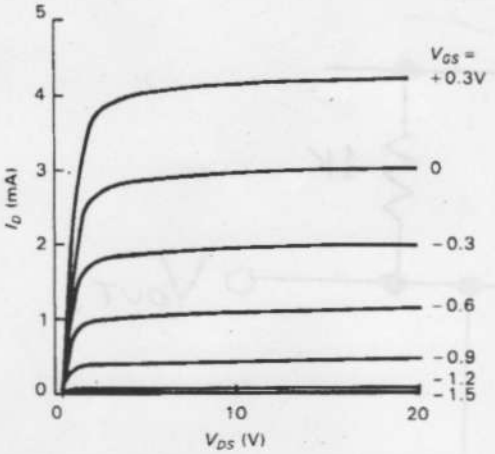
555 timer overview (from Wikipedia)

Nr.	Name	Purpose
1	GND	Ground, low level (0 V)
2	TRIG	A short pulse high-to-low on the trigger starts the timer
3	OUT	During a timing interval, the output stays at $+V_{CC}$
4	$\overline{\text{RESET}}$	A timing interval can be interrupted by applying a reset pulse to low (0 V)
5	CTRL	Control voltage allows access to the internal voltage divider (2/3 V_{CC})
6	THR	The threshold at which the interval ends (it ends if the voltage at THR is at least 2/3 V_{CC})
7	DIS	Connected to a capacitor whose discharge time will influence the timing interval
8	$V+$, V_{CC}	The positive supply voltage which must be between 3 and 15 V



Pinout diagram

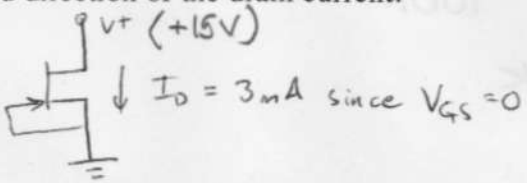
1. (30 points) FETs. Consider the I_D versus V_{DS} curves shown (for various values of V_{GS}) for the 2N5484 n-channel JFET. (You've seen these on your homework and in lab.) In what follows, to receive full credit, your drawings must be clear, complete, and readable.



a) (5 points) Estimate the transconductance of this JFET in its saturated region.

$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \approx \frac{1mA}{0.3V}$ or $3.33 \frac{mA}{V}$ $\left(\frac{1}{300.\Omega}\right)$

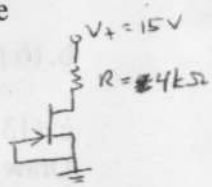
b) (6 points) Draw below a circuit consisting of this JFET with its source at ground, the gate connected to the source, and the drain connected to a power supply V^+ of +15 V; show on your drawing the magnitude and direction of the drain current.



c) (6 points) Now suppose there's a load inserted between V^+ and the drain. Estimate the maximum value of the load resistance R_{load} up to where this circuit remains an adequate current source. (For estimation, let a 10% current deviation be considered adequate.)

max load is found by the condition that the JFET must be saturated
$\Rightarrow V_{DS} > 3V$

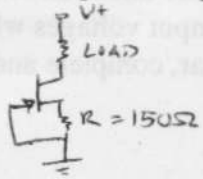
Then $R_{max} = \frac{15V - 3V}{3mA} = 4k\Omega$



d) (7 points) Now suppose you'd like a different current than that in part c. Design and carefully draw, showing values of components, a single +15 V power-supply JFET current source delivering 2 mA through a load.

$I_D = 2mA \Rightarrow V_{GS} = -0.3V$

$\rightarrow R = \frac{0.3V}{2mA} = 150\Omega$



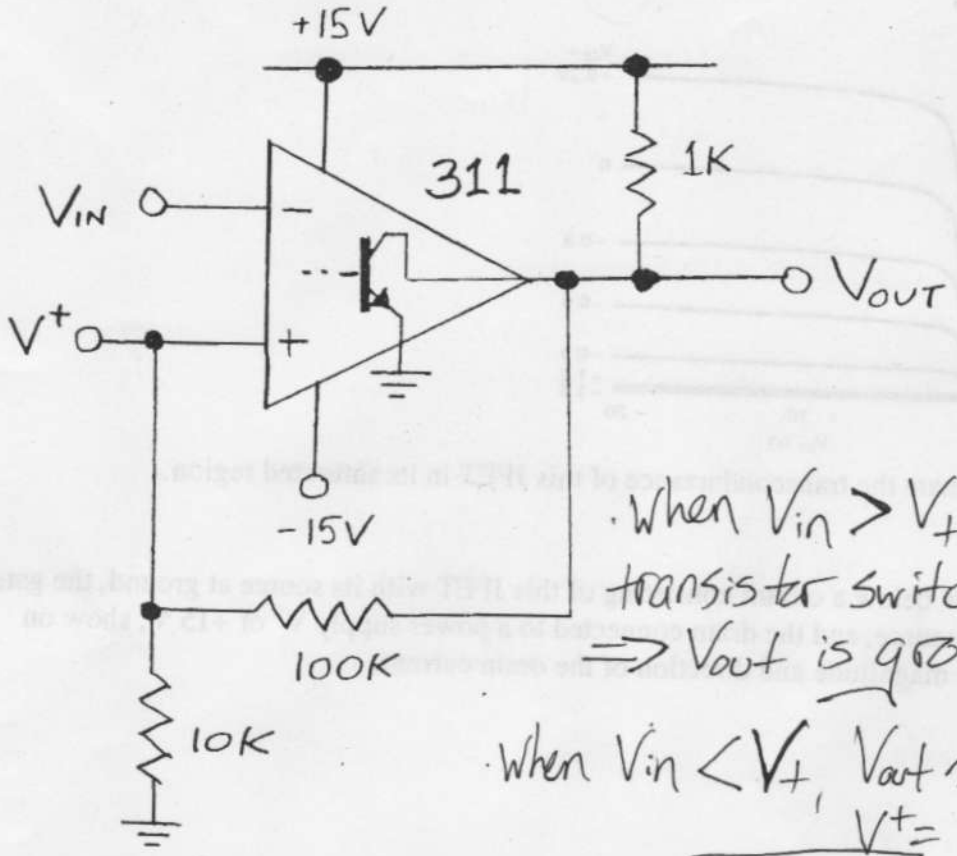
e) (6 points) Now suppose the load in part d is 50 Ω: Estimate the minimum value of the power supply voltage V^+ down to where the circuit is still an adequate 2 mA current source. (For estimation, let a 10% current deviation be considered adequate.)

$V_{DS,min} \approx 3V$. Then $V^+_{min} = V_{DS} + V_{GS} + I R_{LOAD}$

$= 3V + 0.3V + (.002)(50)$

$= \boxed{3.4V}$

2. (25 points) 311 comparator. Consider the following circuit containing the 311 comparator. (Recall the 311 is not an op-amp, it has an open-collector output) V^+ is a test-point where you'll measure a voltage.



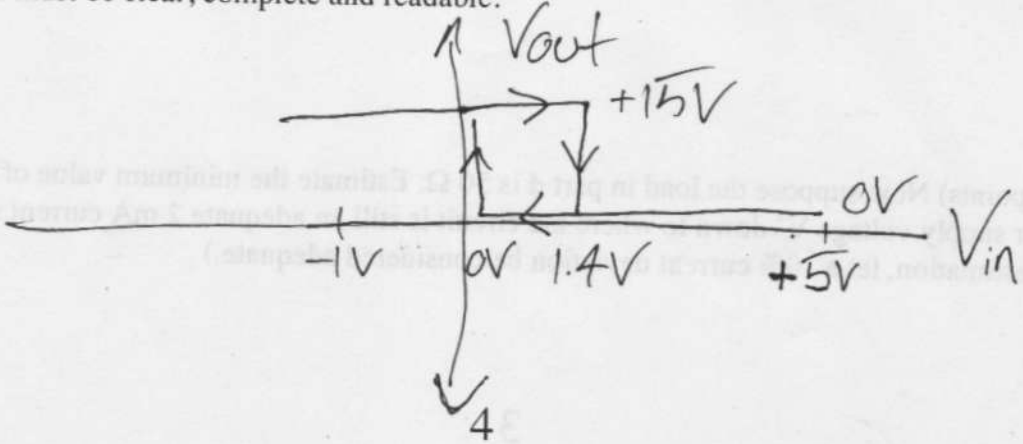
- When $V_{in} > V_+$, the transistor switch is "on" $\Rightarrow V_{out}$ is grounded.
- When $V_{in} < V_+$, $V_{out} \approx 15V$

$$V^+ = V_{out} \cdot \left(\frac{10}{110}\right) \approx 1.4V$$

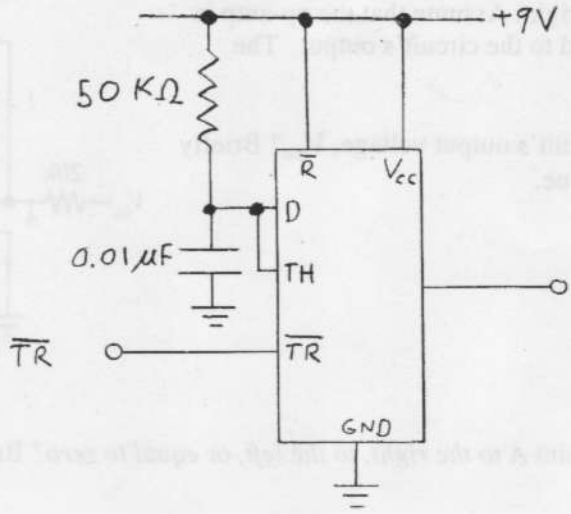
a. (6 points) When Vin = +15 V, what's V_{out} and V^+? $V_{out} = 0V$ $V^+ = 0V$

b. (6 points) When Vin = -15 V, what's V_{out} and V^+? $V_{out} = +15V$ $V^+ = 1.4V$

c. (13 points) Consider an input-voltage excursion of V_{in} from -1 V to +5 V then back to -1 V. Draw below the hysteresis curve for this excursion. That is, make a careful quantitative plot of V_{in} on the horizontal axis and V_{out} on the vertical axis for this excursion. Where the plot has hysteresis, indicate the direction of the excursion with arrows. Be careful to indicate on the plot the values for input voltages where the output makes transitions. To receive full credit, the plot must be clear, complete and readable.



3. (20 points) 555 timer. Consider this 555 timer circuit:

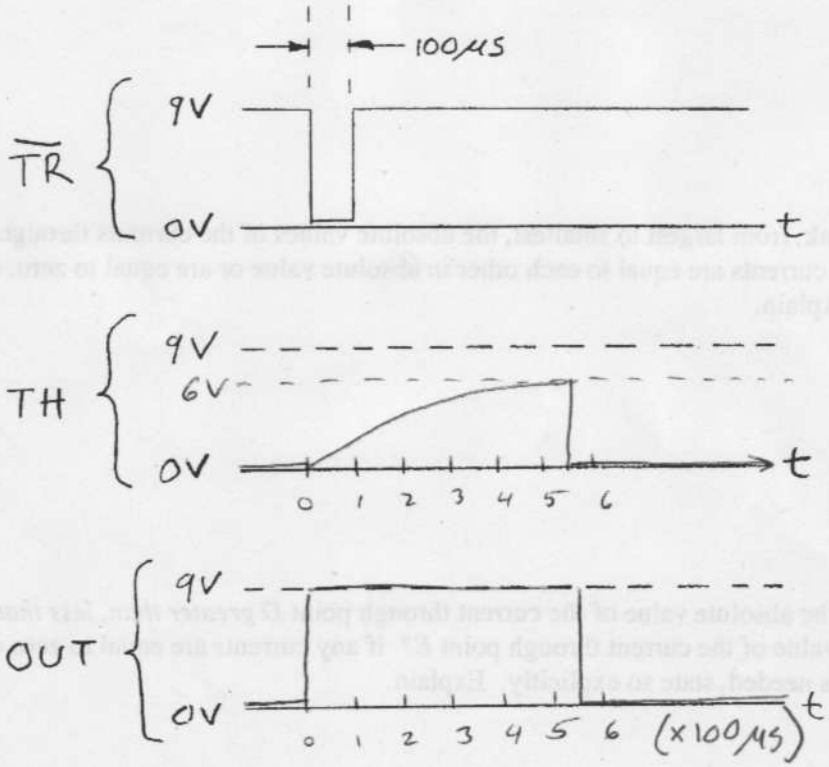


$\tau = RC = 500\mu s$

$V_{TH}(t) = 9(1 - e^{-t/\tau}) = \frac{2}{3}V_{cc} = 6$

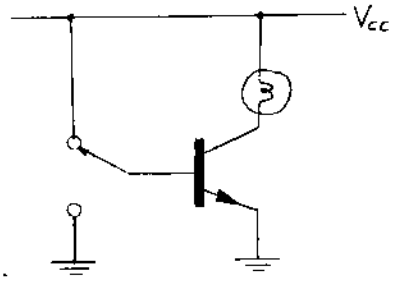
$\Rightarrow t \simeq 550\mu s$

A negative pulse of width 100μs is applied to the trigger input, as shown below. Draw the corresponding curves for the output (OUT) and the voltage at the threshold input (TH) and discharge pin (D) versus time. The curves should have the correct scale in time (as set by the timing and width of the trigger input pulse) and voltage (using the voltage scales given).

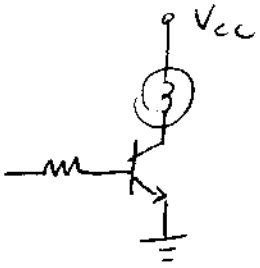


3. (25 points total) "Bad circuits." Each circuit below has a serious fault that makes it "bad". To the right of each circuit, (i) explain in 10 words or less (no more) why the circuit is bad and, (ii) sketch the corresponding corrected "good" circuit. need: (i): 3, & (ii): 3

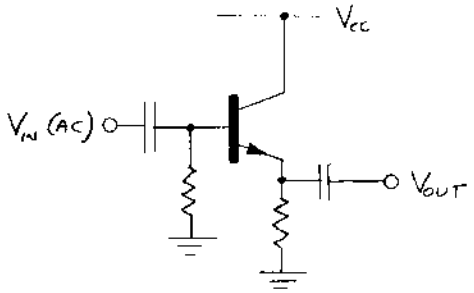
a. (6 points) Transistor-switch driving a light-bulb



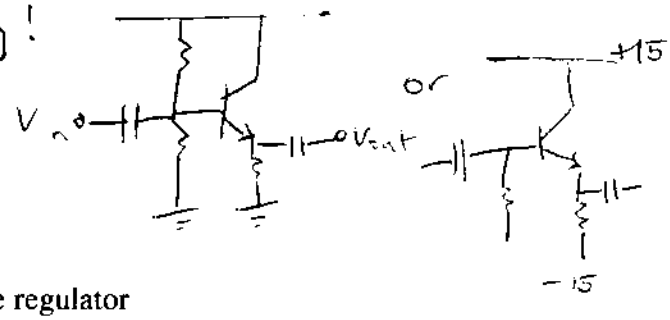
I_B unlimited!



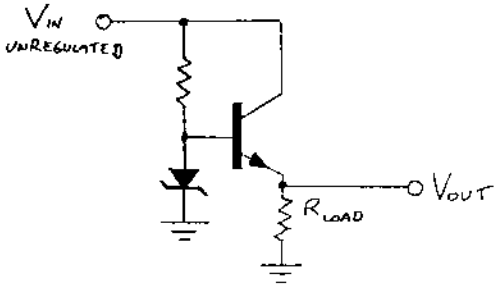
b. (6 points) Follower with AC-coupled input and output



clipping!

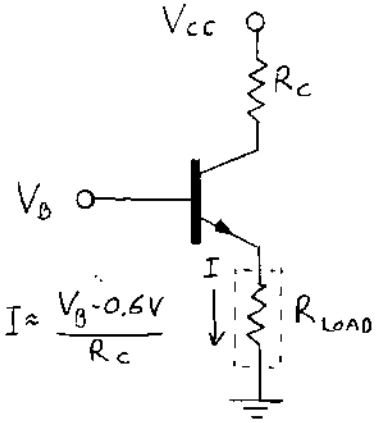


c. (6 points) Zener-diode and emitter-follower voltage regulator



diode backwards!

d. (7 points) Current source (from fixed voltage V_B) through a varying load R_{load}



$R_C \longleftrightarrow R_{LOAD}$!