

# Physics 334

## Notes for Lab 5 – Transistors II and FETs

February 10, 2009

For this week: Lab manual sections **5-6, 7-1, 7-2a, 7-3a, 5.2;**

5-6 Here we look at the push pull follower. This type of output is fairly common with power amplifiers because it burns less power (and therefore produces less heat and uses up batteries much slower). Can you see how the push-pull follower got it's name?

This circuit has a bit of a problem for many applications as designed. If you're an audio enthusiast you've heard of the "crossover distortion" that you'll see when you look at the output.

If you have have high frequency oscillations on this circuit (makes your signal look "fuzzy"), note the trick about putting a 470 ohm resistor (and if needed a small capacitor) to stabilize the circuit. What type of filter are you making if you do add this?

Check your transistors quickly before wiring this circuit for a  $V_{BE}$  drop in the appropriate direction. Also, watch for high currents when you turn on your power supply... If you see lots of current, you've probably got your transistors miswired or swaped. Shut the supply off immediately and make corrections.

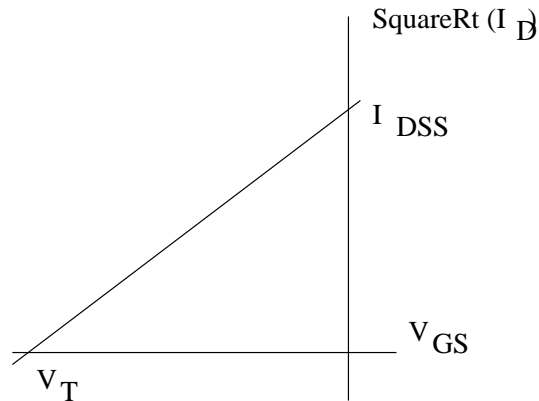
7-1 Do as directed. Test 2 2N 5485 and keep track of which is which so you can compare  $I_{DSS}$  and  $V_T$  Use the fluke meter (300mA scale) to measure  $I_D$ . Because  $V_{DS} = 15V$ , the FET is in the "saturation region so we expect:

$$I_D = C(V_{GS} - V_T)^2 \text{ where } C = \frac{V_{DSS}}{V_T^2} \quad (1)$$

Ignore the question about text 3.15. Instead make two tables (one for each FET) like the following:

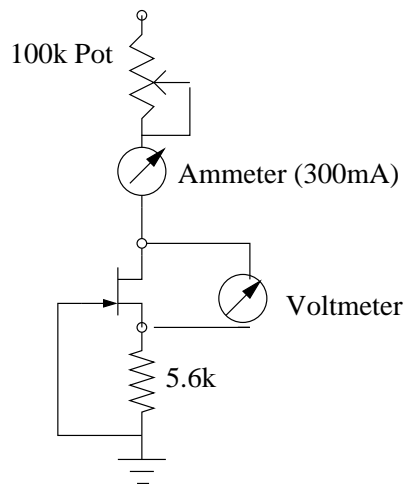
$V_{GS}$ Volts	$I_D$ (mA)	$\sqrt{I_D}$

And plot  $\sqrt{I_{DS}}$  vs.  $V_{GS}$ . You should get something akin to the the following. Note  $I_{DSS}$  – The Y axis intercept.



7-2a Measure  $V_{DS}$  and  $I_D$  simultaneously – The diagram should probably have explicitly shown the DMM to measure voltage – though you know how...

You probably already figured it out... In any case, it should look like:



7-3 Do as instructed.

You may find yourself unhappy with complications from biasing, non-linearity and so forth with your transistor circuits. Turns out, that made other people unhappy in the past, too. Next week, you'll learn how we can make many things better by using feedback.

You don't need to worry about all the details after "You can do better" on p. 159. However, the general result is important. The FET transconductance is not perfect... and this leads to a voltage attenuation in a follower circuit due to  $1/g_m$ . And this limitation is significant in some cases... Looking like a pesky resistor of hundreds of ohms or more. The bipolar transistor has a similar limitation, which you'll explore next if you get time.

5-2 Remember from your study of common emitter amplifiers that the gain is  $Gain = -\frac{R_{Collector}}{R_{Emitter}}$ . A naive application of this might lead you to believe that if you could make the emitter resistance small enough, you could get any gain you wanted... Even infinite gain.

Not so. Here we push the common emitter amp to its limit by giving it an emitter impedance that looks to be almost zero at signal frequencies. What is the impedance of the parallel combination of the resistor and capacitor at the emitter at DC? At a signal frequency of 10kHz?