Phys. 334

Day 5 Lecture Notes

Real Op-amps vs. Ideal Op-amps:

Last week, we considered ideal op-amps, and implicitly assumed that an ideal op-amp has the following properties:

1.) Infinite input impedance (ie the inputs draw no current)
2.) Zero output impedance (at least very small)
3.) Zero common mode gain (V_{out} independent of ($V_+ + V_-$))
4.) Zero offset voltage ($V_{out} = 0$ when $V_+ = V_-$)
5.) Infinite slew rate (output can change instantaneously)
6.) No temperature dependence or power supply voltage dependence
7.) Infinite voltage gain at all frequencies

These assumptions made it easy to understand op-amp circuits via the 2 Golden Rules. Real op-amps have limitations and we need to examine them to know when to expect simple picture to break down. We will look at each assumption in turn and then see some consequences in circuit examples.

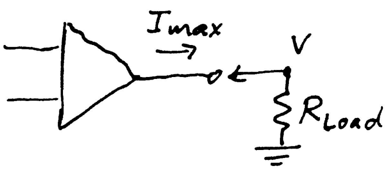
1.) Op-amp inputs are the bases of transistors (or the gates of Field Effect Transistors, FETS, another type of transistor). The input impedance ranges from $10^6\ \Omega$ for bipolar input transistor op-amps to $10^{12}\ \Omega$ for FET input op-amps (like the LF411 that you use in the lab). This value is so high that the input impedance ($\Delta V_{in}/\Delta I_{in}$) can be dominated by the input capacitance, $C_{in} \approx 10$ pF.

For FET input op-amps, Z_{in} is high enough to be considered ideal. Even so, there is a related characteristic, the input bias current, I_B, that you need to be aware of. A small current flows into or out of each input. This is the current associated with biasing the input stage to its operating region, and is nearly the same for the + and – inputs. For bipolar input transistor op-amps, $I_B \approx 10$ nA, while for FET inputs, $I_B \approx 50$ pA (like the LF411).

The major consequence of I_B is that you must always provide a path for these currents to flow and when they do flow through resistors, they create a small voltage difference that can alter the DC value of V_{out}. (This is why we added the 1 MΩ resistor to V_+ for the current to voltage converter circuit on page 4-6 of last week's notes.)

2.) Without feedback, op-amps have an output impedance of ≈ 100 Ω. With negative feedback that senses the output voltage (as was the case for all of the circuits last week), Z_{out} is reduced to about 0.1 Ω. This is small enough to consider as ideal.

A more serious limitation is that the maximum output current that an op-amp can provide is only ≈ 20 mA. If your op-amp is driving a load resistance and you want its output to swing between + and – 10 Volts, for example, then you need $I_{max} \times R_{Load} > 10V$ which means that R_L must be greater than 500 Ω, even though $Z_{out} \approx 0.1\Omega$. To increase the output current, one uses a transistor connected to the output (eg the power booster we saw last week).



$$V_{max} = I_{max} \times R_{Load}$$

$$R_{Load} \geq \frac{V_{max}}{I_{max}}$$

3.) The common mode gain for op-amps is usually negligible, that is, close to ideal. A more practical consideration is that the common mode voltage, $(V_+ + V_-)/2$, is usually limited to be between zero and 3 or 4 Volts away from the power supply voltage:

$$-V_{EE} + 3V < (V_+ + V_-)/2 < V_{CC} - 3V$$

4.) Because of small differences between the + and – inputs, $V_{out} \neq 0$ when $V_+ = V_-$. Instead, $V_{out} = 0$ when $V_+ - V_- = V_{OS}$, where V_{OS} is the 'offset voltage": $V_{out} = \text{Gain} \times (V_+ - V_- - V_{OS})$

V_{OS} ranges from 1 µV to 1 mV for different op-amps (≈ 1 mV for the LF411) and typically 2 of the pins on the op-amp chip are provided to allow you to trim this offset to zero. With negative feedback, the effect of V_{OS} is often negligible.

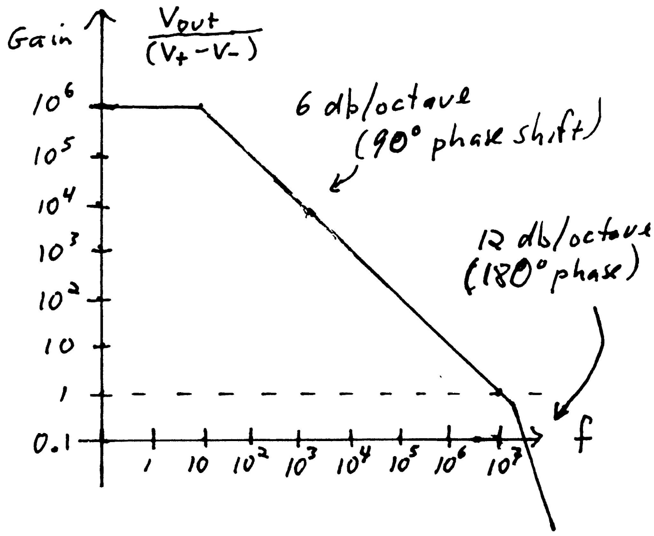
5.) Because of capacitance within the op-amp and the ability to provide limited current, $(dV/dt)_{max} = I_{max}/C$, that is, the output voltage cannot change faster than a finite rate.

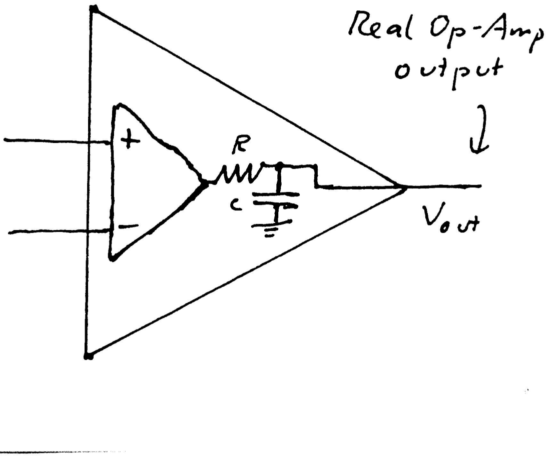
$(dV_{out}/dt)_{max}$ is called the slew rate and ranges from 1 V/µs to 100 V/µs depending on the op-amp. (It is ≈ 10 V/µs for the LF411). Its main effect is to limit the amplitude of output voltages at high frequencies: If $V_{out} = A\sin(\omega t)$, then $(dV_{out}/dt)_{max} = \omega A \leq$ slew rate, or

$$A \leq (\text{slew rate})/\omega.$$

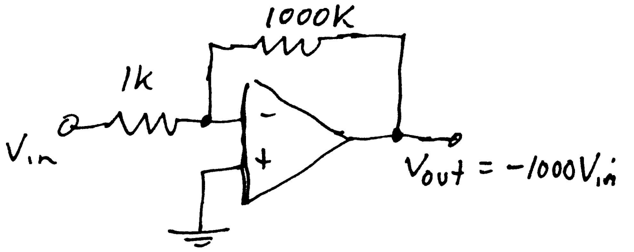
6.) Except for high precision circuits, we can usually neglect the effects of moderate temperature changes on op-amp performance. Similarly, their behavior is not strongly influenced by the value of the power supply voltage (as long as it is within the manufacturer's specified range, typically 8 - 20 Volts).

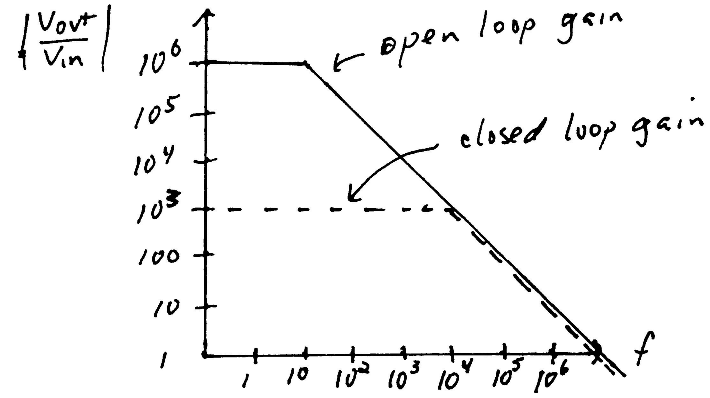
7.) The most serious limitation of op-amps and one that cannot be neglected is the voltage gain vs. frequency. At high enough frequencies, current flows through internal capacitance within the op-amp (which changes the phase of V vs. I by 90°). Two such phase changes gives 180°, which converts negative feedback to positive feedback and the output will oscillate. To prevent such oscillations, op-amp designers have added a low pass filter to the op-amp output to guarantee that the voltage gain is less than 1 at the frequency where the output is phase shifted by 180°. (This is sufficient to suppress oscillations.) The voltage gain vs. frequency of the op-amp then looks like the Bode Plot to the right: the gain is very high at DC and constant up to around 10 Hz. At higher frequencies, the gain falls by 6 db per octave (same as a low pass filter) and reaches 1 at around 10 MHz. Note, between 10 Hz and 10 MHz, the output is shifted in phase by 90° with respect to the input, but this is still sufficient for negative feedback.





There are two important consequences of this reduction of gain vs. frequency. The first is that the maximum gain of a circuit is reduced at high frequencies. For example, an inverting amplifier with a gain of 1000 at DC will only have that gain up to a frequency where the op-amp open-loop gain (gain without feedback) is still greater than 1000. In the Bode plot below, the gain would fall from 1000 after 10 kHz by 6 db per octave. (If you need higher gain, say at 100 kHz, you could use 2 op-amps and multiply the gains together.)





The second consequence of the gain vs. frequency reduction is that you must be careful not to add an additional 90° phase shift in the feedback circuit (to add to the 90° from the op-amp output). Sometimes, stray capacitance between wires acts with resistors in the circuit to form a low pass filter and give an additional 90° phase shift, and your op-amp becomes an oscillator. The cure is to wire neatly and make sure your grounds are well-defined.

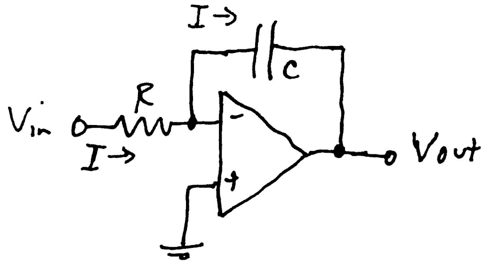
Additional op-amp circuits:

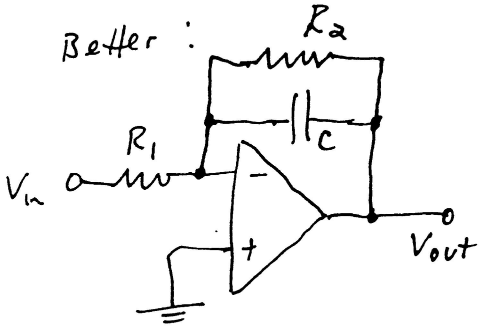
Integrator: Recall that a low pass filter made an integrator as long as $V_{out} << V_{in}$. An op-amp does a much better job.

As before, $V_- = V_+ = 0$, making $V_{in} = I/R$

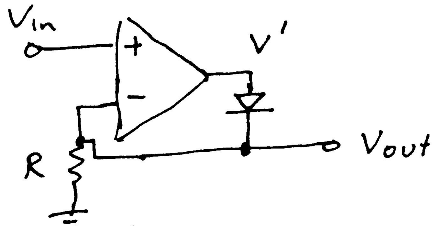
and $I = CdV_{out}/dt$, giving $V_{out} = -\int V_{in}dt/RC$

A problem is that even for $V_{in} = 0$, V_{OS} and I_B will cause V_{out} to ramp up or down to saturation. The solution is to add a large resistor in parallel with C. For frequencies above $1/(2\pi R_2 C)$, $Z_C < R_2$ (ie the current flows through C) and the circuit acts like an integrator. For $f < 1/(2\pi R_2 C)$, $R_2 < Z_C$ and we have our inverting amplifier, ie the output is small for $V_{in} = 0$. (R_2 provides negative feedback for DC voltages.)



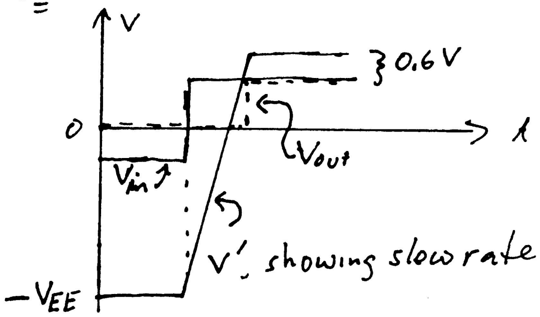


Op-amp Rectifier: We can make a nice rectifier, without the 0.6 Volt diode drop, with an op-amp. When the diode is on, there is negative feedback and $V_{out} = V_- = V_{in}$, and the diode is on when current flows through it, which means $V_- = V_+ > 0$.

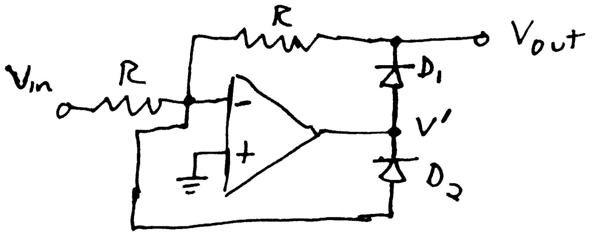


The diode is off and there is no negative feedback when $V_- = 0$, which happens when $V_{in} < 0$ ($V' < 0$).

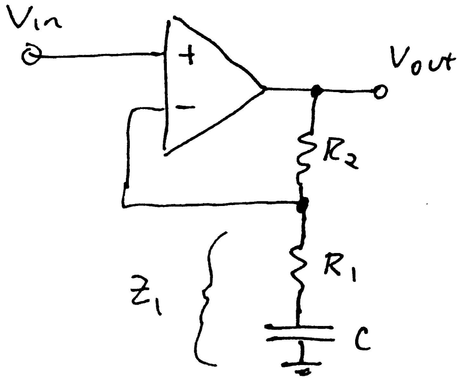
A problem with this circuit is that when $V_{in} < 0$, the op-amp output, V' swings to $-V_{EE}$, say −13 Volts. The instant V_{in} becomes > 0, V' has to swing all the way from $-V_{EE}$ to V_{in} and because of the finite slew rate, that takes some time and there will be a small delay between V_{out} and V_{in}, as shown to the right.



A solution is to use another diode to prevent V' from going into saturation, as shown to the right. Here, when $V_{in} < 0$, current flows to the left through both R's (D_1 is on) and we have our inverting amp with $R_1 = R_2 = R$, giving $V_{out} = -V_{in}$. When $V_{in} > 0$, current flows to the right and D_2 is on, making $V' = -0.6$ Volt and because D_1 is off, no current flows through the feedback R, making $V_{out} = 0$. So here, we have an inverting rectifier and because $V' = -0.6$ Volts when $V_{in} > 0$, it takes a much shorter time for V' to reach +0.6 Volts when V_{in} crosses to < 0.



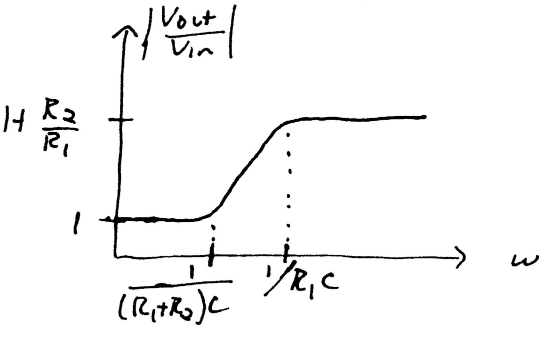
Amplifier with frequency dependent gain: We can achieve different voltage gains at different frequencies by using capacitors as well as resistors in the feedback loop. We need only remember to provide some negative feedback at all frequencies. For example, to have a gain of 1 at low frequencies and a gain of 100 at high frequencies, we could do the following:



$$\frac{V_{out}}{V_{in}} = 1 + \frac{R_2}{Z_1} = 1 + \frac{R_2}{R_1 + 1/j\omega C}$$

$$\frac{V_{out}}{V_{in}} = 1 + \frac{j\omega R_2 C}{1 + j\omega R_1 C} \quad \begin{array}{l} \to 1 \text{ at } \omega = 0 \\ \to 1 + \frac{R_2}{R_1} \text{ at } \omega > \frac{1}{R_1 C} \end{array}$$

$$\frac{V_{out}}{V_{in}} = \frac{1 + j\omega(R_1+R_2)C}{1 + j\omega R_1 C}$$



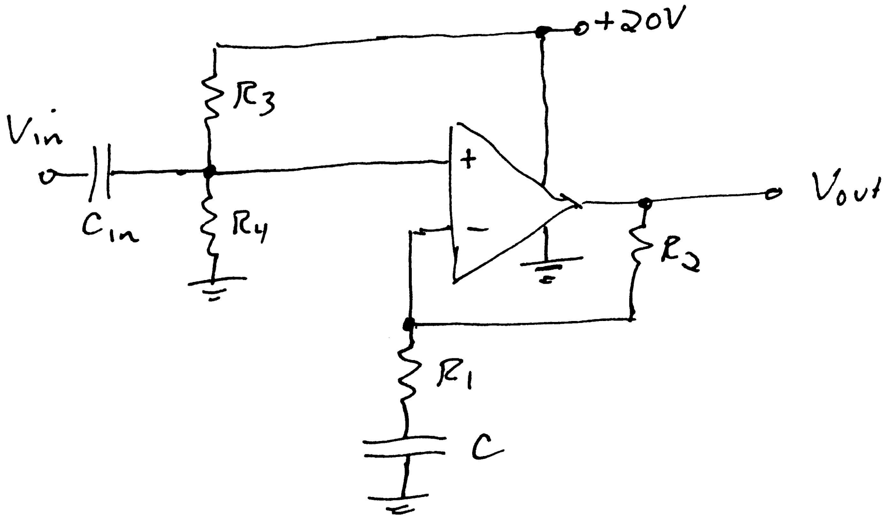
Op-amp with one power supply: We can operate op-amps with a single power supply, say +20 Volts, by biasing the output to half way between, say 10 Volts. (Bias means the value when the input is zero.)

In the circuit below, the feedback loop has a DC gain of 1 and a signal frequency gain of $1 + R_2/R_1$ as derived on the previous page.

R_3 and R_4 form a voltage divider, making $V_+ = 20\ R_4/(R_3 + R_4) = V_{out}$ at DC because the gain is 1.

A signal frequencies, we get a gain of $1 + R_2/R_1$ centered around V_{out} at DC.

C_{in} is a blocking capacitor, allowing the input voltage to be centered around a voltage other than that given by the voltage divider.



Useful for battery operated devices where the battery provides a single voltage.