COUNTERS, CONTINUED

USE COUNTERS AS A DESIGN TOOL TO MEASURE SOME QUANTITY

1. Make a counter
2. Add gates / flops to start & stop
3. MAKE CIRCUITRY TO CONVERT Quantity of interest into a pulse
4. USE COUNTER TO MEASURE LENGTH of PULSE

EXAMPLE — DIGITAL VOLTMETER (H & H)

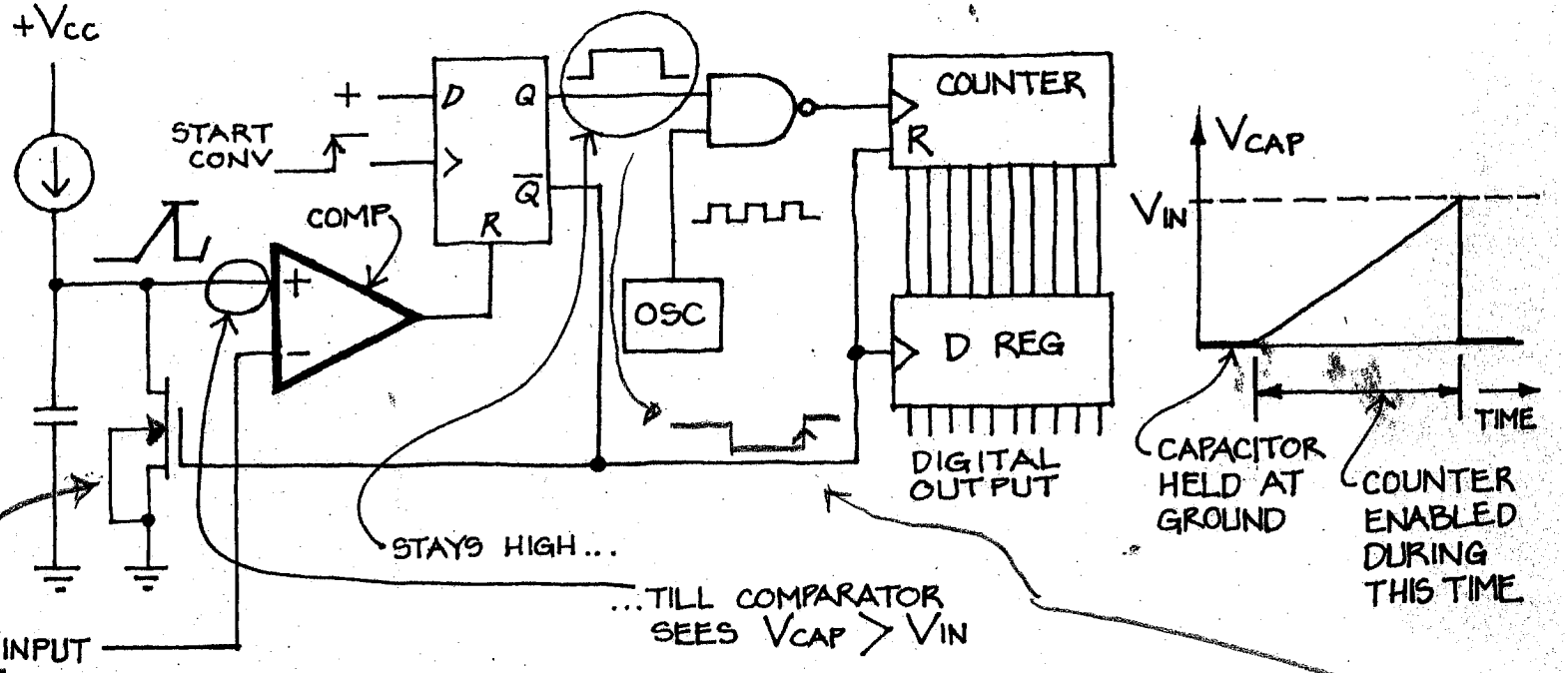


Figure N15.14: Example 1: measure period to measure *voltage*

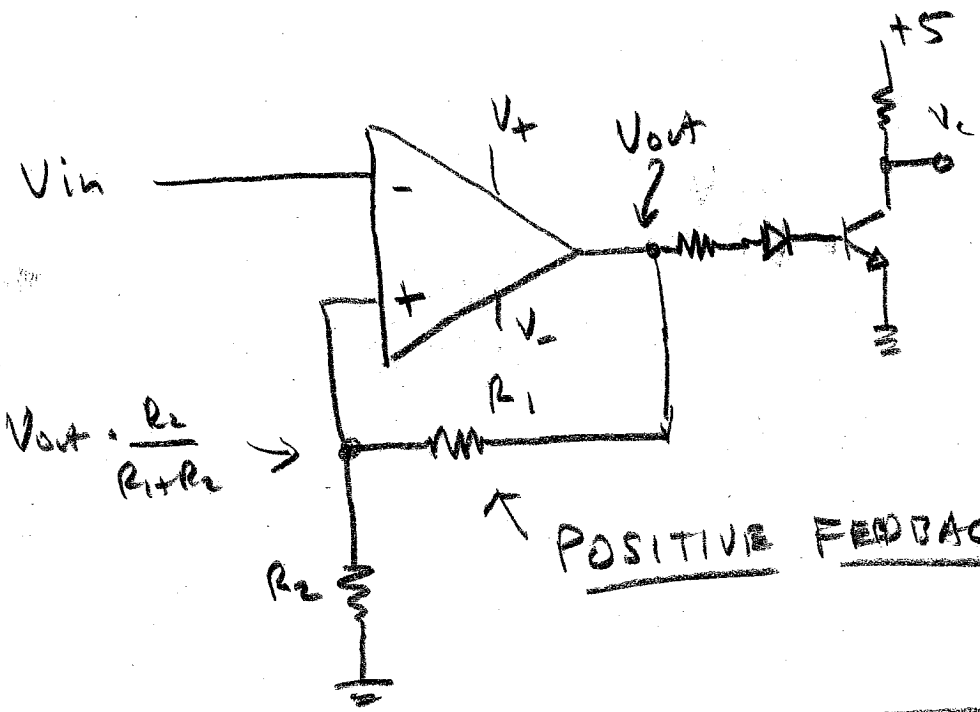
MEASURED VOLTAGE GOES HERE

TRANSISTOR NORMALLY ON — SHORTS OUT CAPACITOR

$\overline{Q}$ → LO TURNS FET OFF, VOLTAGE ON CAP RISES LINEARLY.

RISING EDGE LATCHES COUNT AND RESETS COUNTER

NOTE : A COMPARATOR IS AN OP-AMP DESIGNED TO HAVE A TWO-STATE OUTPUT, ONLY DETERMINES IF $V_+ > V_-$ or $V_+ < V_-$



BECAUSE GAIN OF OPAMP IS SO HIGH

$V_{out} = V_-$ IF

$V_{in} > V_- \cdot \frac{R_1}{R_2+R_1}$

TRANSISTOR OFF

$\Rightarrow V_c = +5$

WHEN $V_{in} < V_- \frac{R_1}{R_1+R_2}$

V_{out} SWINGS TO V_+

TURNING TRANSISTOR ON, $V_c \to \approx 0$

NOTE THRESHOLDS DIFFER

GOING LOW → HIGH, $V_+ \frac{R_1}{R_1+R_1}$

HIGH → LOW $V_- \frac{R_1}{R_1+R_2}$

HYSTERESIS

SIMILAR CIRCUIT USED TO MEASURE CAPACITANCE. RECALL 555 TIMER

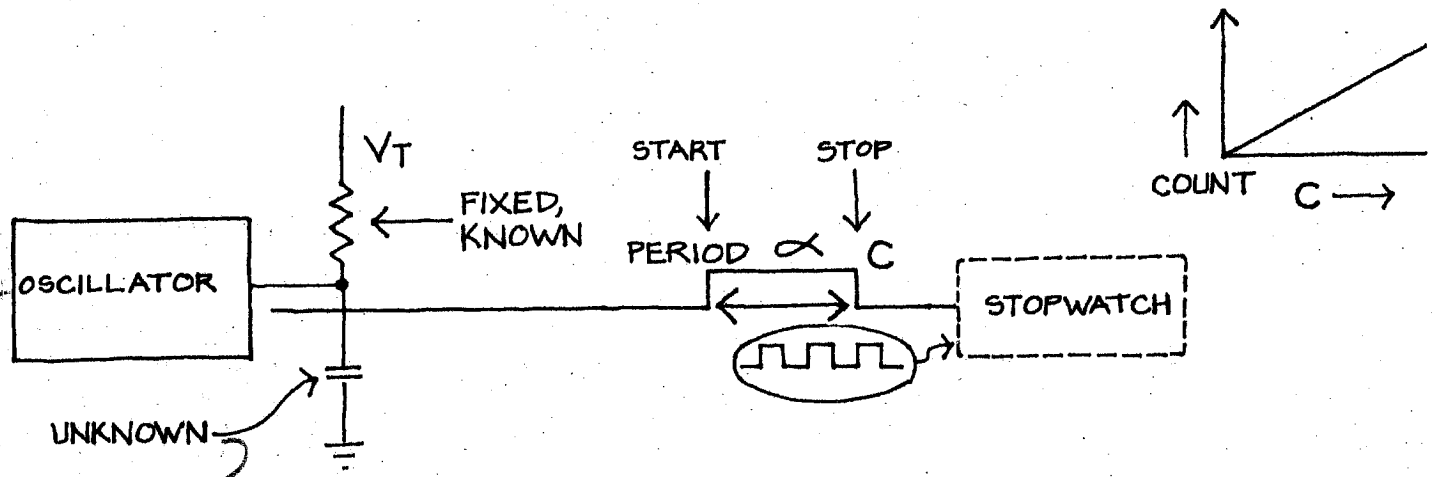
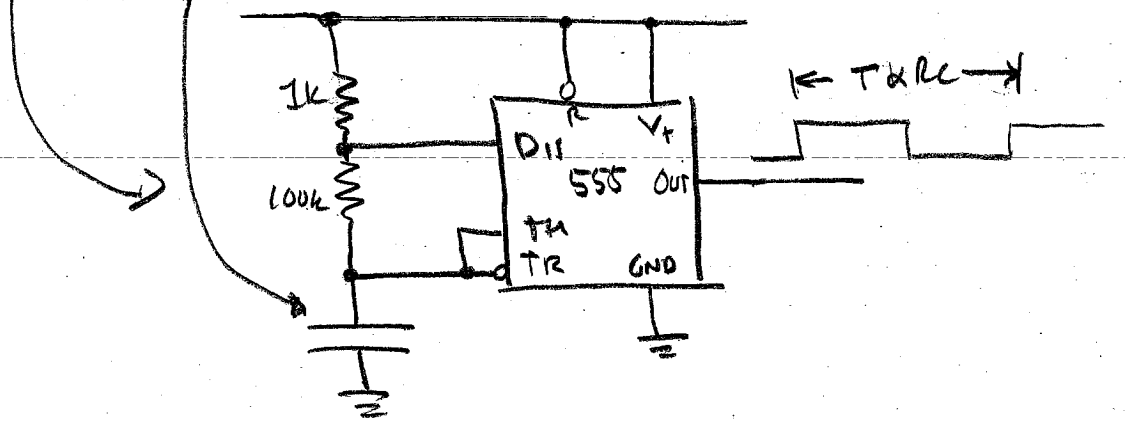
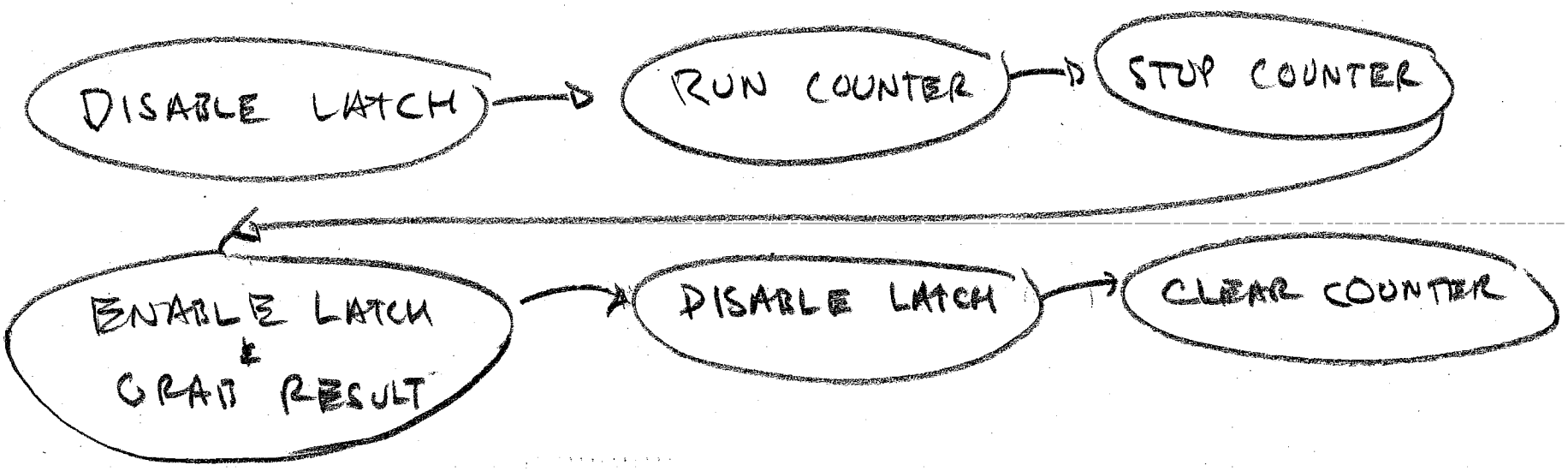


Figure N15.15: Example 2: measure period to measure *capacitance*



PERIOD PROPORTIONAL TO CAPACITANCE

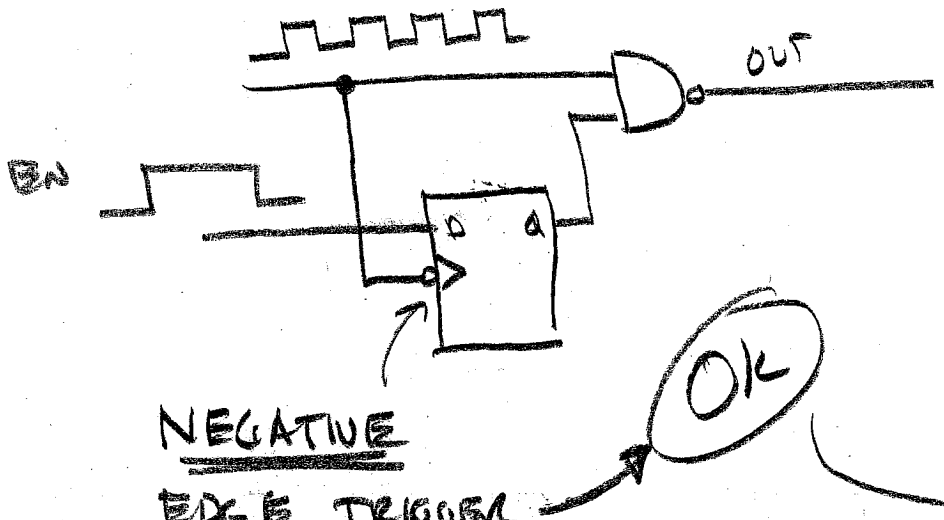
BASIC SEQUENCE OF COUNTING:



TIMING OF ENABLE PINS & CLOCK EDGES IS CRITICAL.

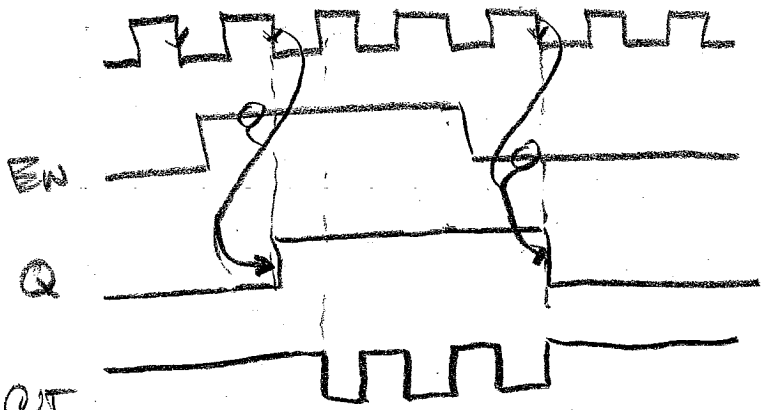
- PAY ATTENTION TO POS (_F_) OR NEG (_L_) EDGE TRIGGERS
- PAY ATTENTION TO POSITIVE OR NEGATIVE ASSERTIONS
- PAY ATTENTION TO PROPAGATION DELAYS

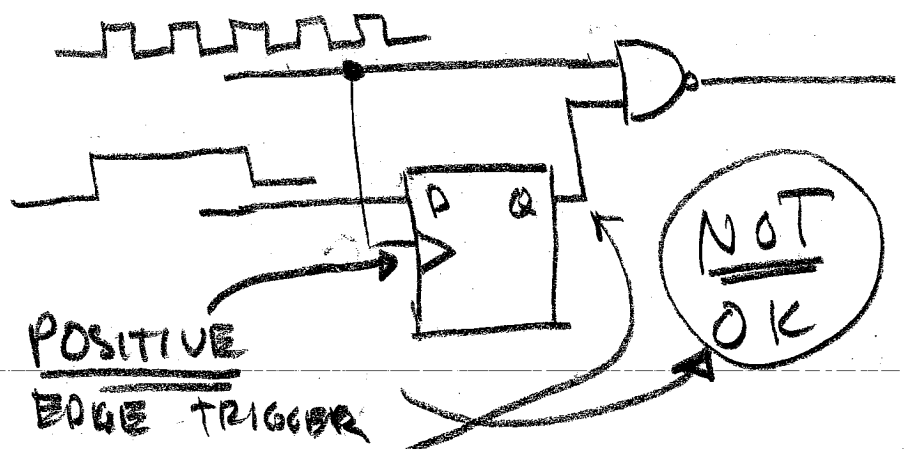
EXAMPLE PROBLEM — PULSE SYNCHRONIZER



NEGATIVE EDGE TRIGGER

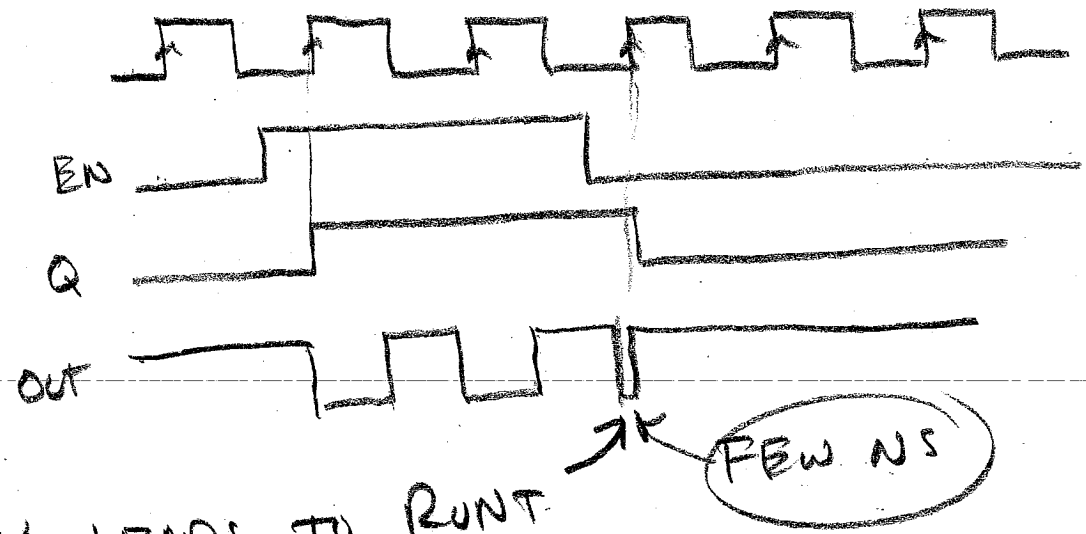
OK





POSITIVE EDGE TRIGGER

NOT OK



PROPAGATION DELAY LEADS TO RUNT

SAME PROBLEM – ANOTHER CONTEXT

÷13 COUNTER

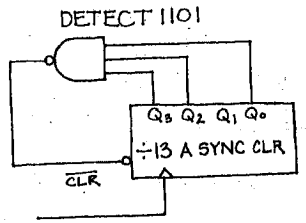


Figure X15.1: A poor way to convert natural binary counter to + 13

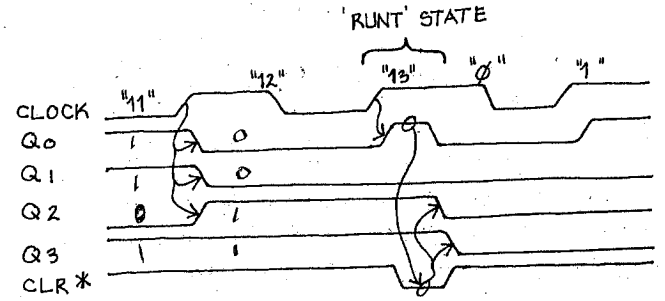


Figure X15.2: Poor " + 13" design: false *14th* state between 12 and 0

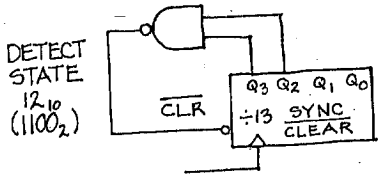


Figure X15.3: Synchronous + 13 from + 16 counter

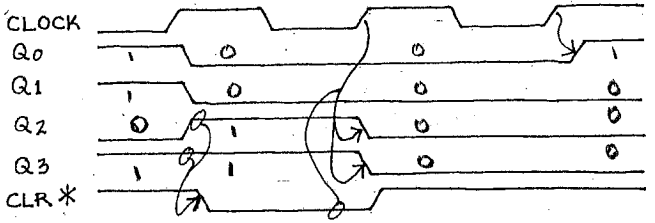
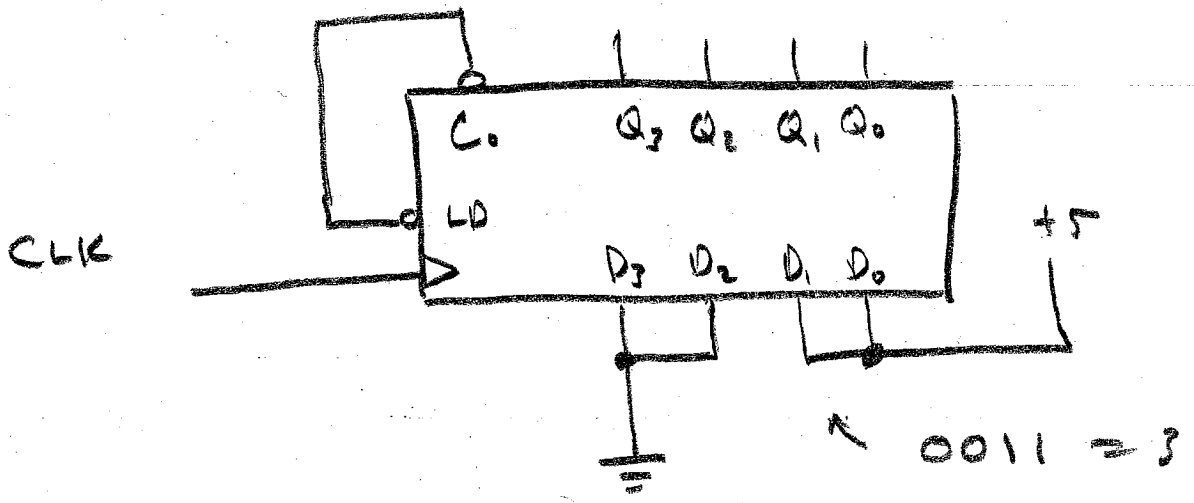


Figure X15.4: Proper count modification: using synchronous Clear*

÷13 COUNTS 0, 1, 2, ..., 12

ANOTHER WAY TO DO IT – USE SYNCHRONOUS LOAD



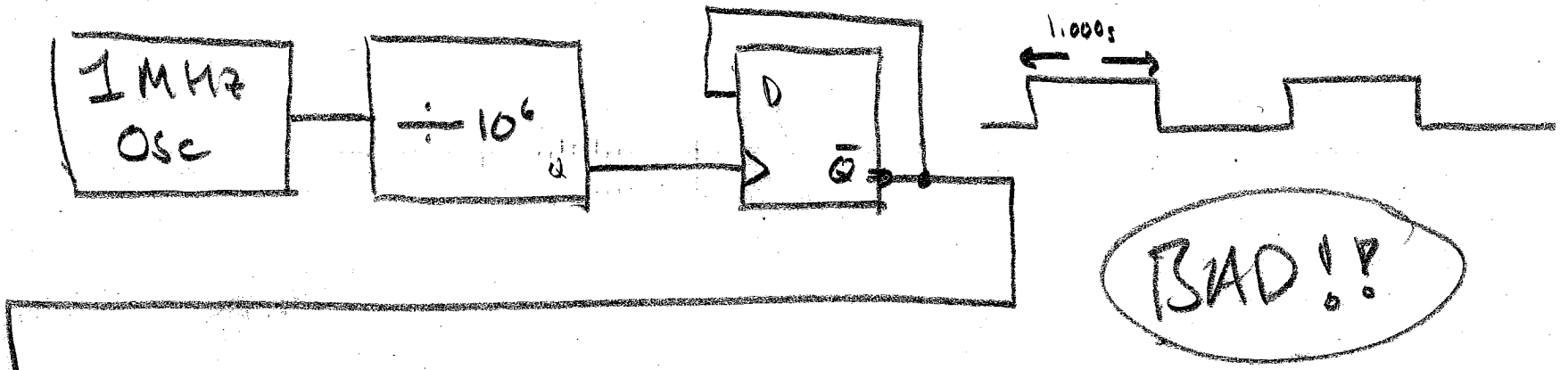
This counts from 3, 4, ..., 15 } 13 states

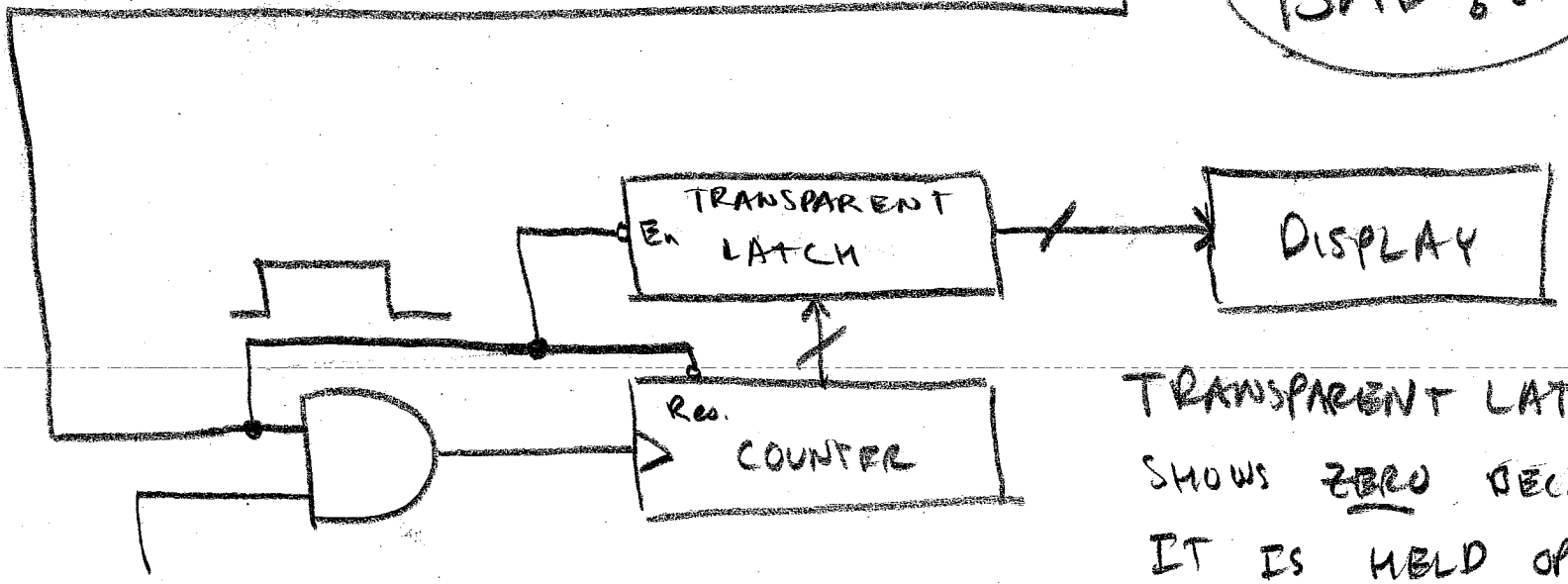
But
- Peculiar numbers (if you care)
- Could count Down (last reversed)

EXAMPLE, GOOD & BAD - FREQUENCY COUNTER

IDEA: FREQUENCY = CYCLES/SECOND.

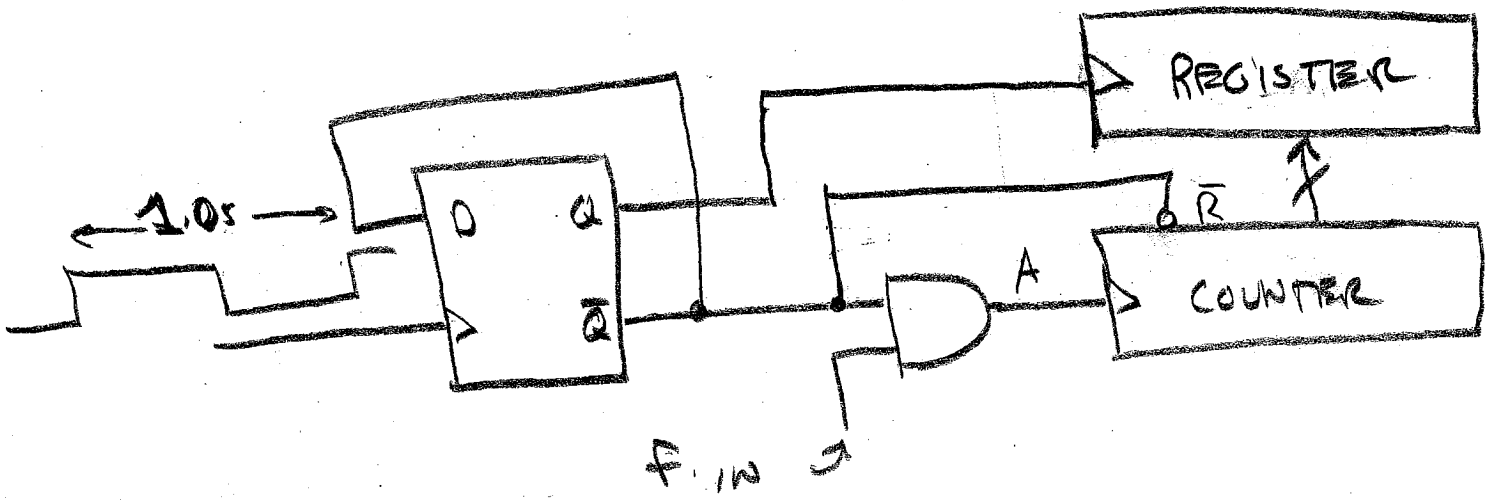
TURN ON COUNTER FOR 1.000 seconds, count CYCLES



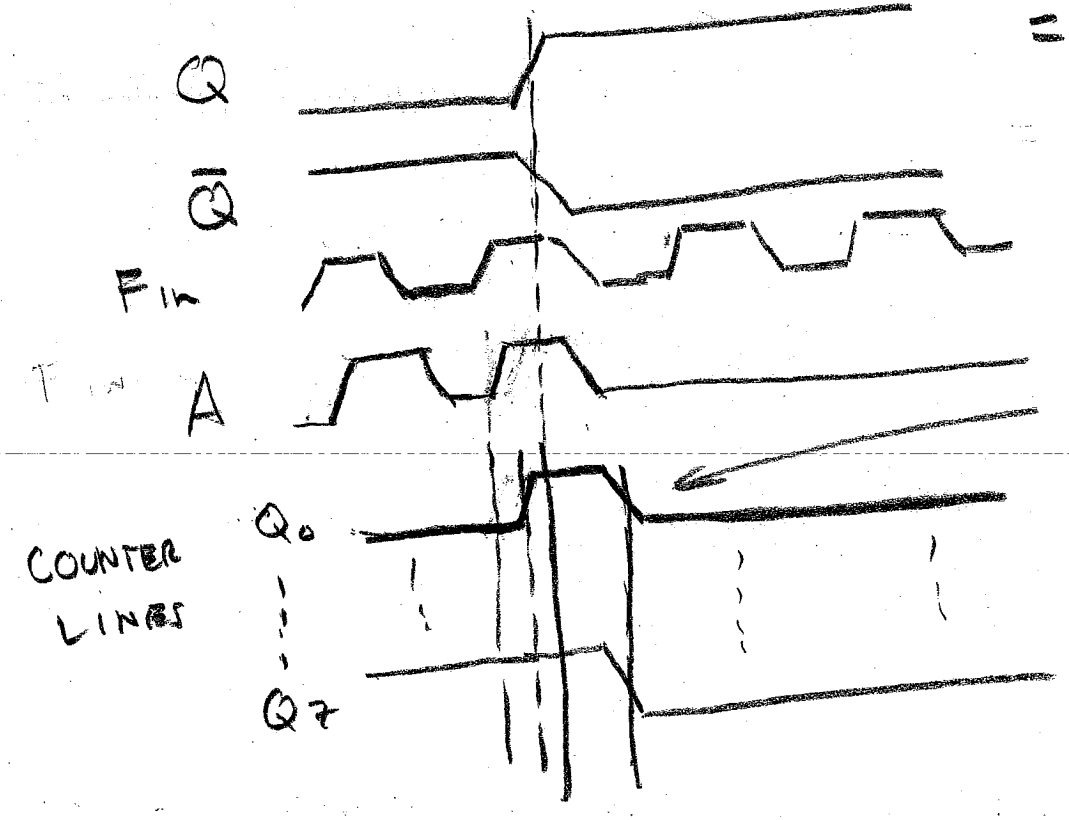


TRANSPARENT LATCH SHOWS ZERO BECAUSE IT IS HELD OPEN ON RESET OF COUNTER

SOLUTION: USE EDGE TRIGGERED REGISTER



= CLOCK INPUT TO REGISTER

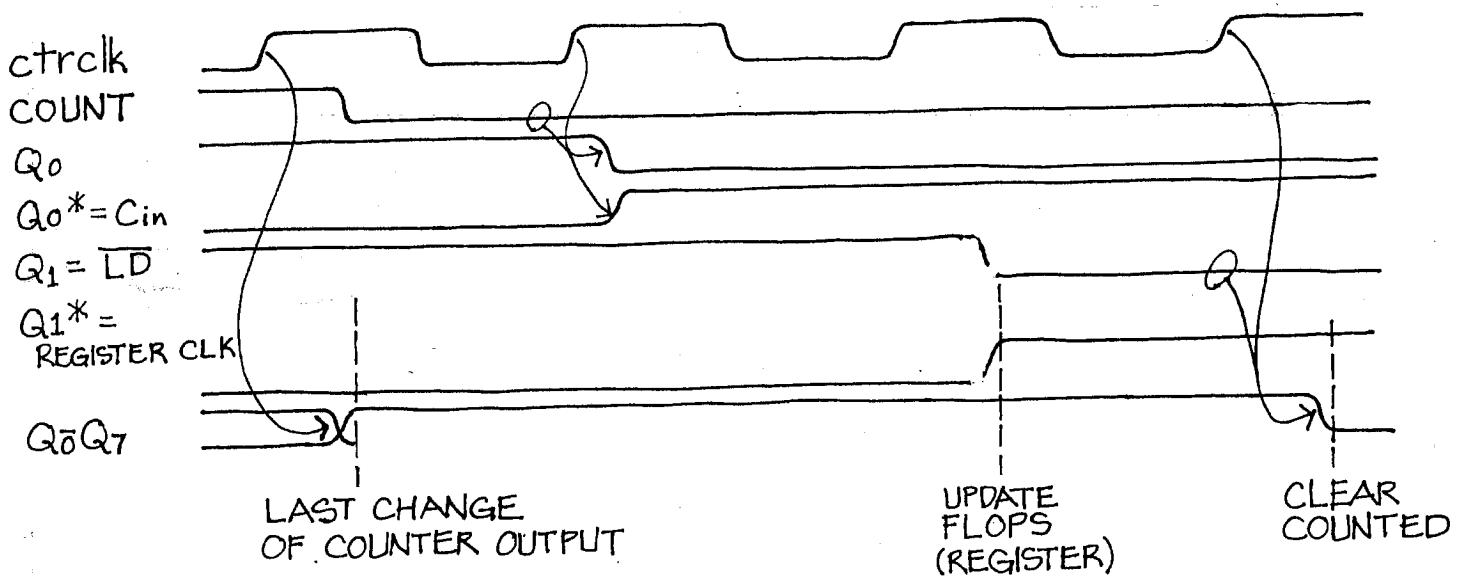


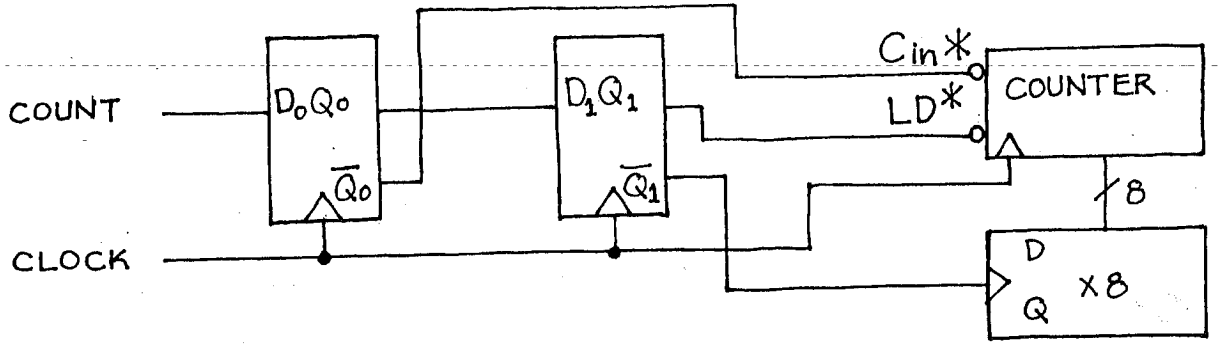
SLIGHT DELAY IN RESET ALLOWS EDGE TRIGGERED REGISTER TO GRAB COUNTS

TIMING TRICKINESS - COUNTER IS STILL COUNTING WHEN REGISTER IS TRIGGERED.

THIS COULD VIOLATE SETUP TIMES OF REGISTER & CAUSE BAD VALUE TO BE RECORDED

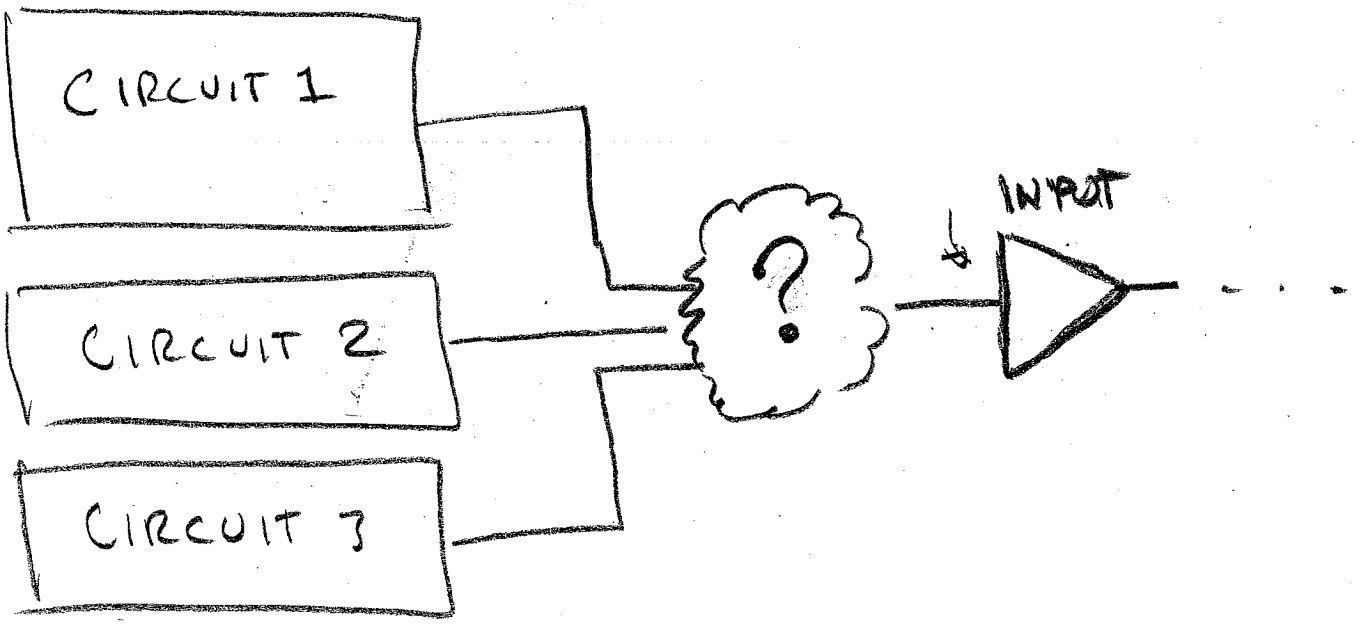
SOLUTION - STOP COUNTER FIRST.



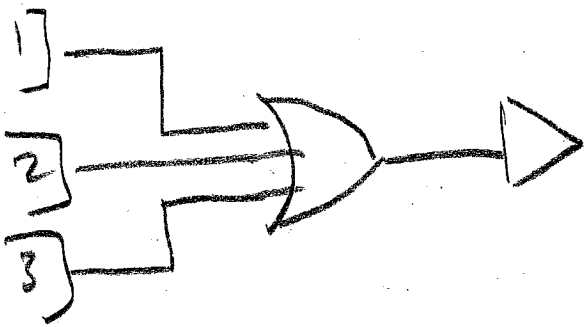


A NEW CONCEPT: THE BUS

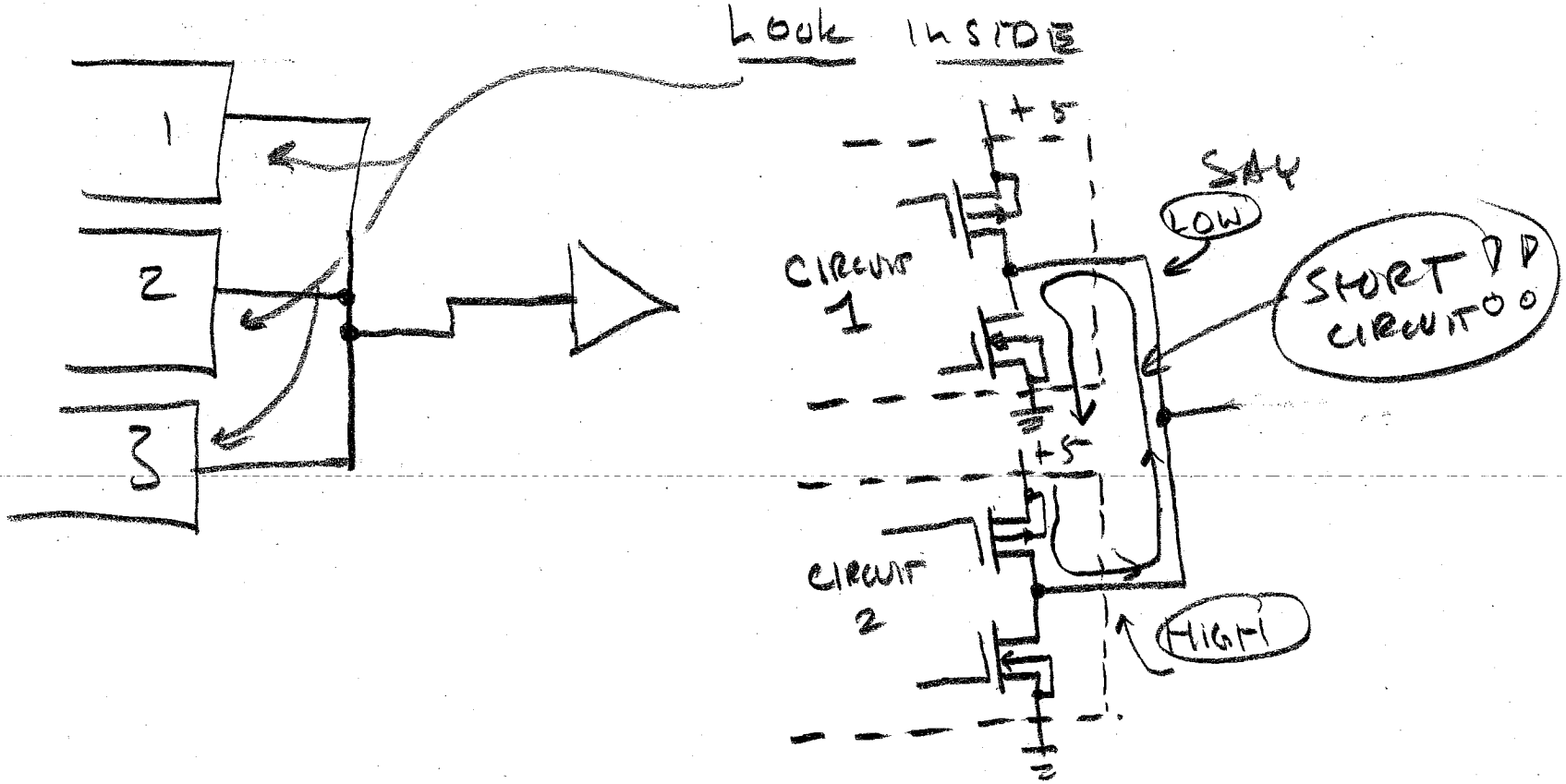
PROBLEM — NOT ENOUGH WIRES OR,
YOU WANT TO HAVE AN INPUT
CHOOSE AMONG VARIOUS OUTPUTS.



ONE POSSIBILITY - OR GATES

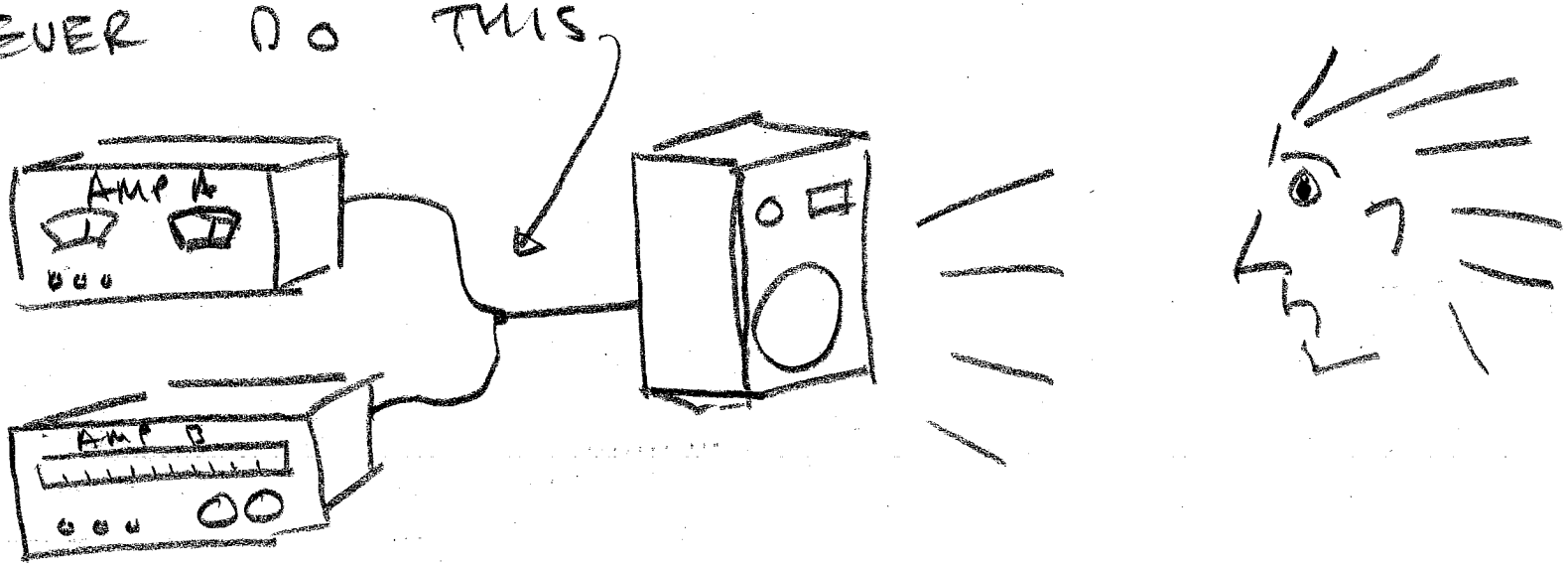


WHY CAN'T THIS HAPPEN?



BRIEF DIGRESSION . . .

NEVER DO THIS



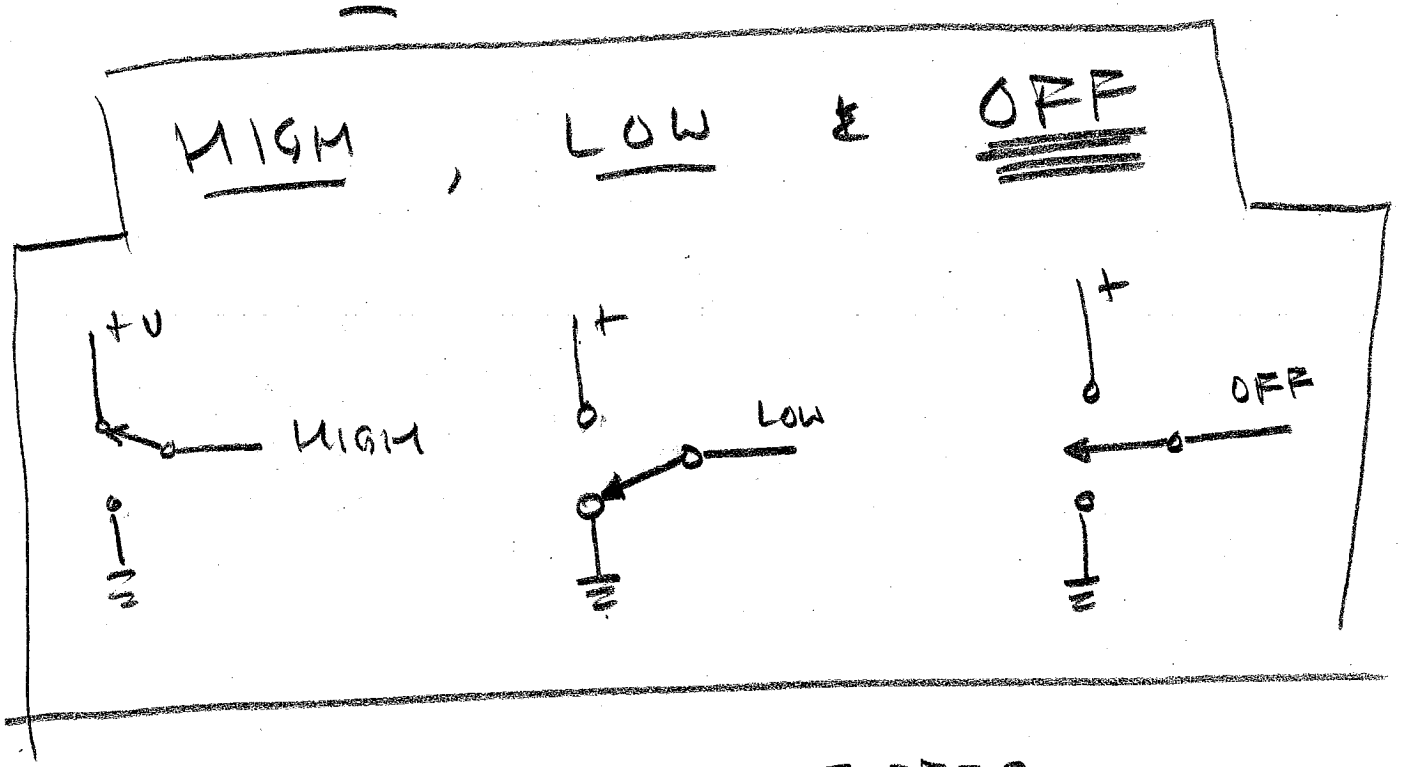
SLIGHT PHASE DIFFERENCE OR VOLUME DIFFERENCE CAUSES AMP A TO BECOME LOAD OF AMP B

POWER AMPS HAVE LOW OUTPUT Z.

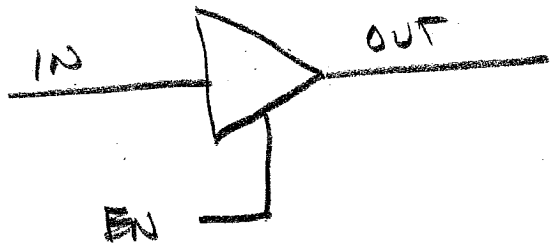
→ RESULT: FRIED AMPLIFIERS

EXTRA OR GATE SOLVES PROBLEM, BUT IS CUMBERSOME.

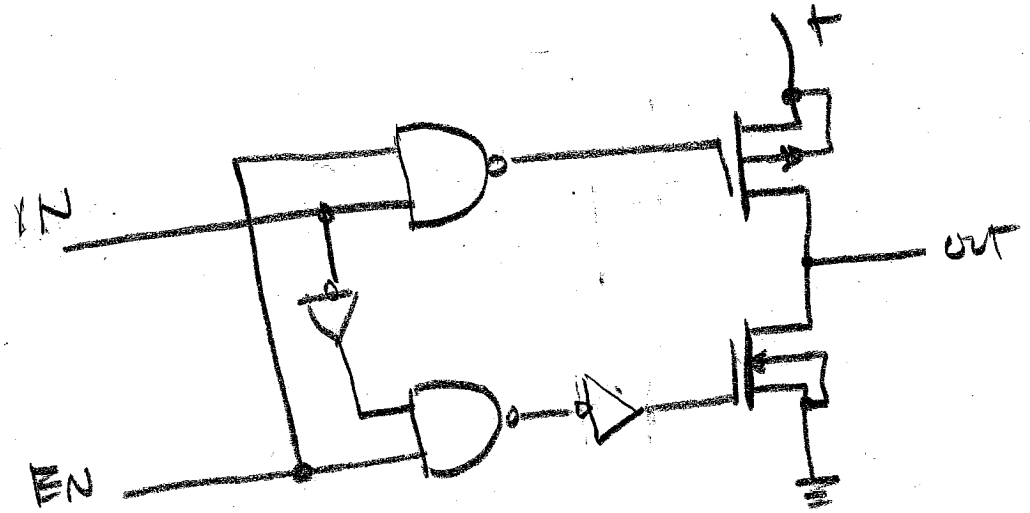
SOLUTION: 3 STATE OUTPUTS



SYMBOL : 3-STATE BUFFER

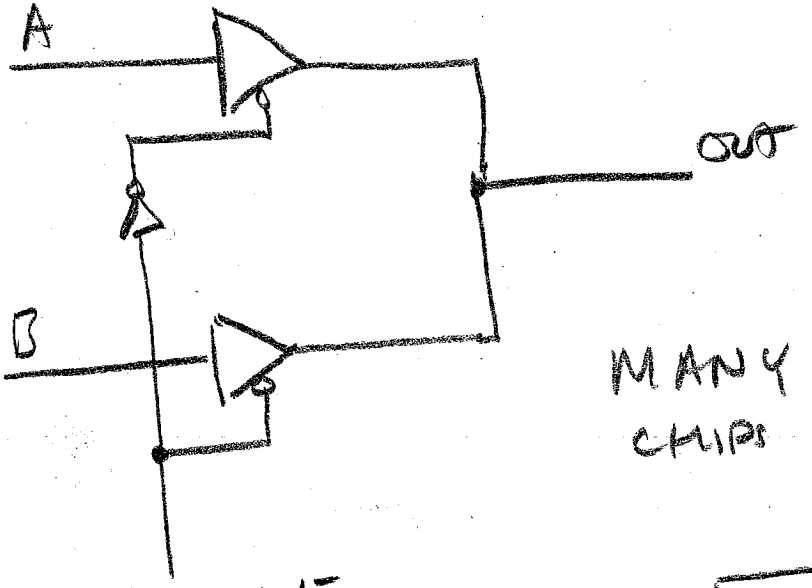


3-STATE OUTPUTS – HOW THEY WORK

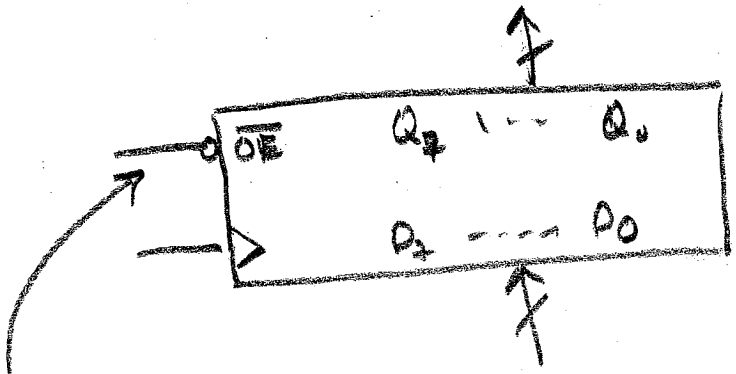


- IF ENABLE IS LOW, BOTH NANDS ARE HIGH, BOTH MOSFETS ARE OFF
- IF ENABLE IS HIGH, MOSFET CORRESPONDING TO IN IS ON → OUTPUT EITHER LOW OR HIGH

WITH 3-STATE OUTPUTS, CAN DO THIS



MANY COUNTERS & REGISTER CHIPS USE 3-STATE OUTPUTS

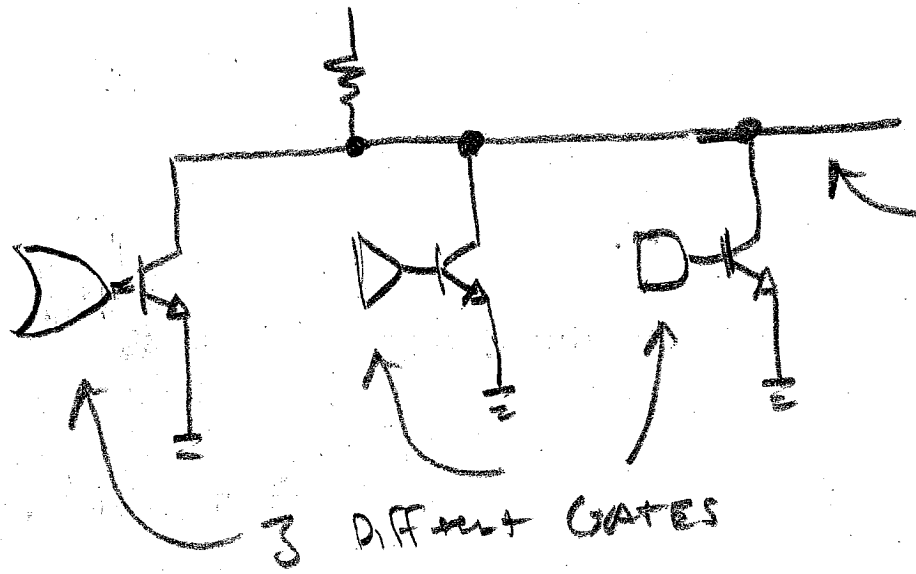


E.G. 74HCS74

MAY BE LABELED { OE = "OUTPUT ENABLE"
CS = "CHIP SELECT"

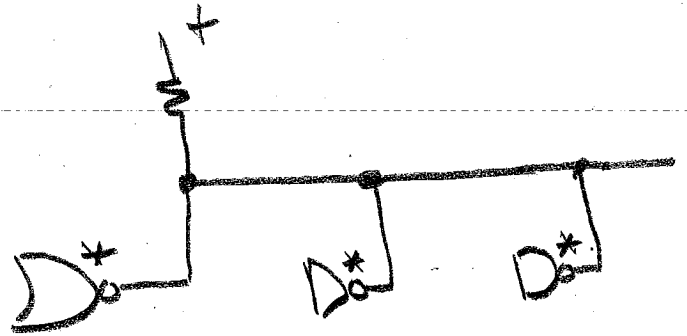
ANOTHER LESS COMMON SOLUTION

"WIRED-OR" OR "OPEN { COLLECTOR / DRAIN }



(Ok) IF MORE THAN 1 ON - ANY ON PULLS OUT LOW.

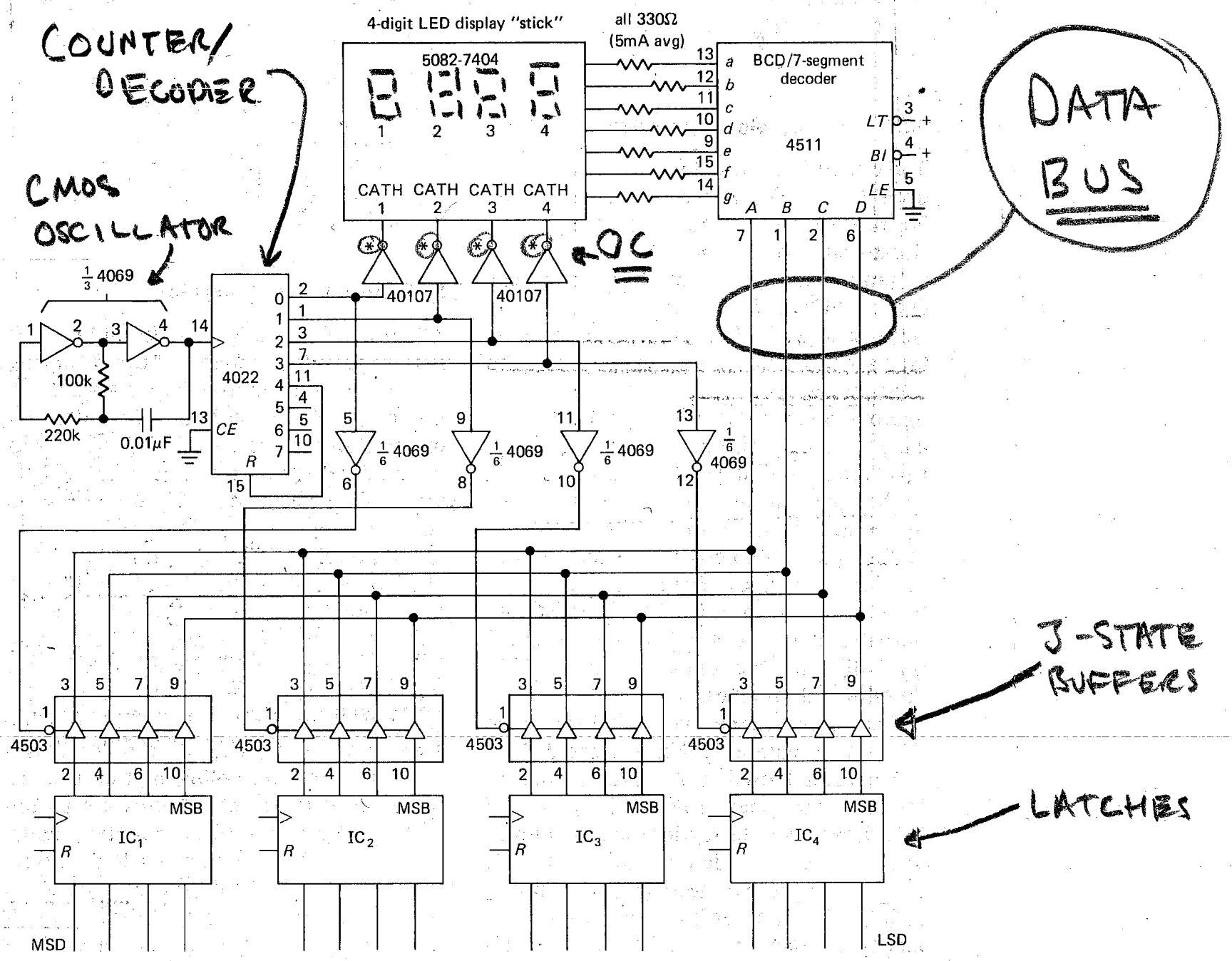
USUALLY DRAWN



NOTE

- PULLUP RESISTOR
- * SYBOL NEAR OUTPUT

EXAMPLE: MULTIPLEXED DISPLAY – USES 3-STATE BUFFERS SO THAT DATA CAN SHARE SAME WIRES



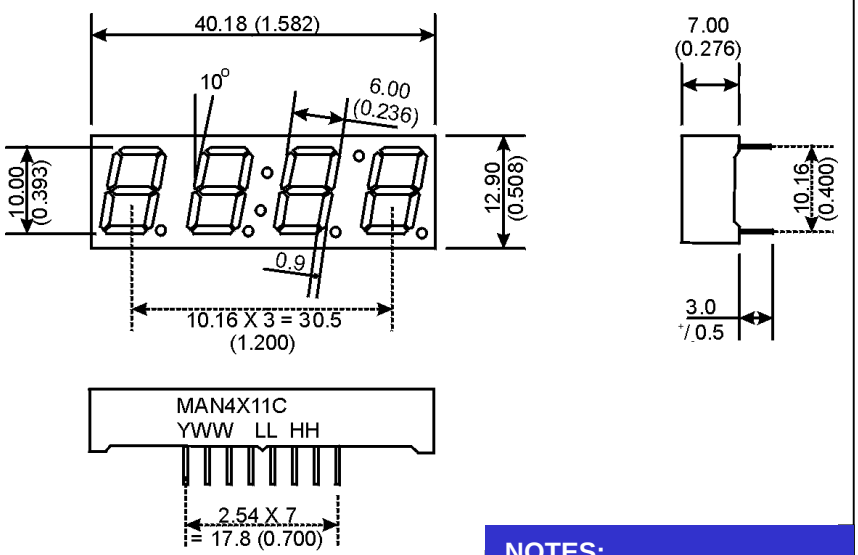
FAIRCHILD
SEMICONDUCTOR™

0.4 Inch (10.2mm) 4 Digit CLOCK STICK DISPLAY

Bright Red MSQC4111C
High Efficiency Red MSQC4911C
Green MSQC4411C

TR/QTS/030800-001

PACKAGE DIMENSIONS



NOTES:

- Dimensions are in mm (inches)
- Tolerances are +/- 0.25 (0.010) unless otherwise stated.

FEATURES

- Bright Bold Segments
- Common Anode/Cathode
- Low Power Consumption
- Low Current Capability
- Neutral Segments
- Grey Face
- Epoxy Encapsulated PCB
- High Performance
- High Reliability

APPLICATIONS

- Appliances
- Automotive
- Instrumentation
- Process Control

MODELS AVAILABLE

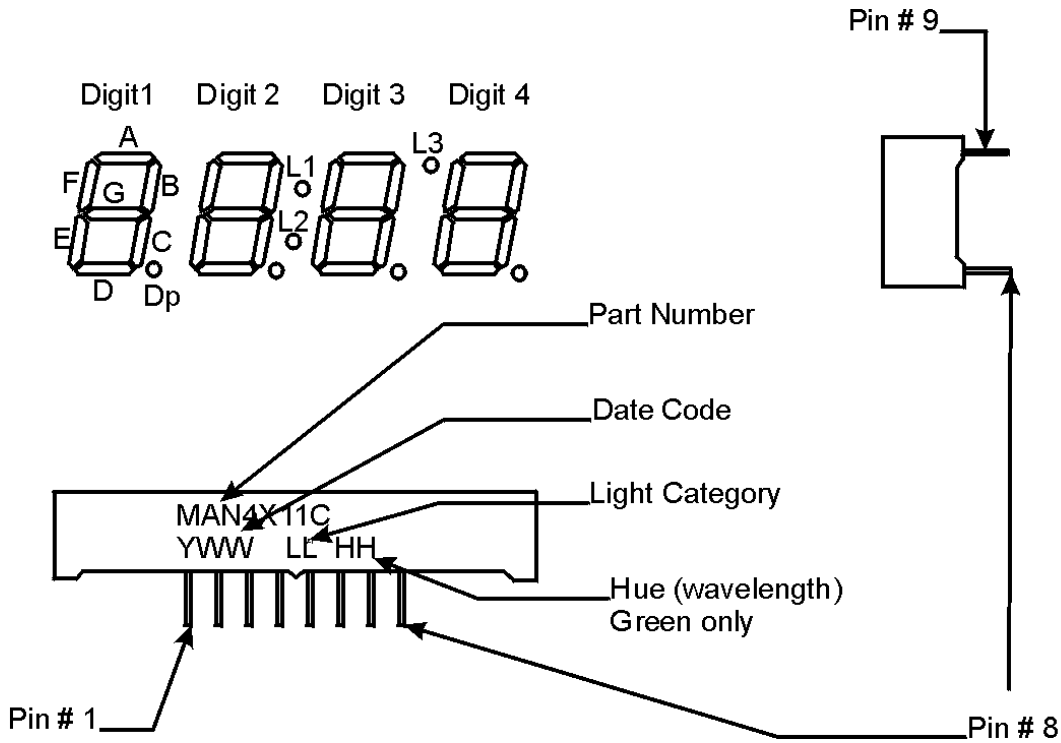
Part Number	Colour	Description
MSQC4111C	Bright Red	Four Digit, 12/24 hour Clock Display, CA
MSQC4411C	Green	Four Digit, 12/24 hour Clock Display, CA
MSQC4911C	High Efficiency Red	Four Digit, 12/24 hour Clock Display, CA

(For other colour/polarity options, contact your local area Sales Manager)

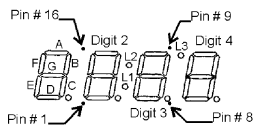
FAIRCHILD
SEMICONDUCTOR™

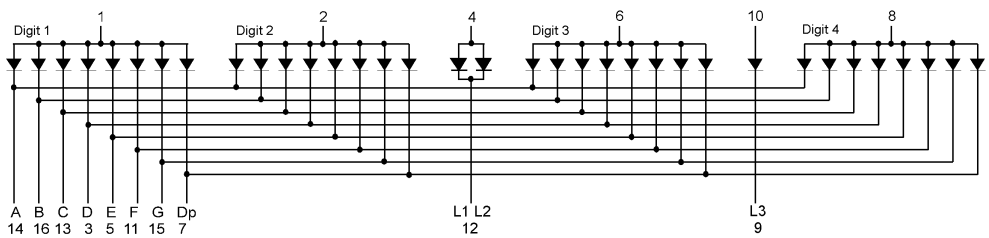
0.4 Inch (10.2mm) 4 Digit CLOCK STICK DISPLAY

PIN ORIENTATION, SEGMENT IDENTIFICATION, AND PRODUCT MARKING



SCHEMATICS





FAIRCHILD SEMICONDUCTOR™

October 1987
Revised March 2002

CD4017BC • CD4022BC
Decade Counter/Divider with 10 Decoded Outputs • Divide-by-8 Counter/Divider with 8 Decoded Outputs

General Description

The CD4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit.

The CD4022BC is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical "1" on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017BC and CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

Features

- Wide supply voltage range: 3.0V to 15V
- High noise immunity: 0.45 V_{DD} (typ.)
- Low power Fan out of 2 driving 74L
  TTL compatibility: or 1 driving 74LS
- Medium speed operation: 5.0 MHz (typ.)
  with 10V V_{DD}
- Low power: 10 μW (typ.)
- Fully static operation

Applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

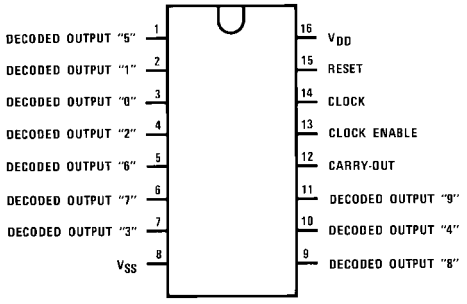
Ordering Code:

Order Number	Package Number	Package Description
CD4017BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4017BCSJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
CD4017BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
CD4022BCM	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
CD4022BCN	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

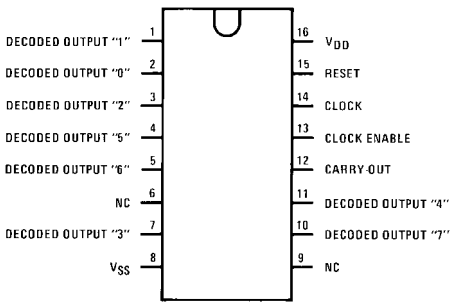
Connection Diagrams

Pin Assignments for DIP, SOIC and SOP
CD4017B



Top View

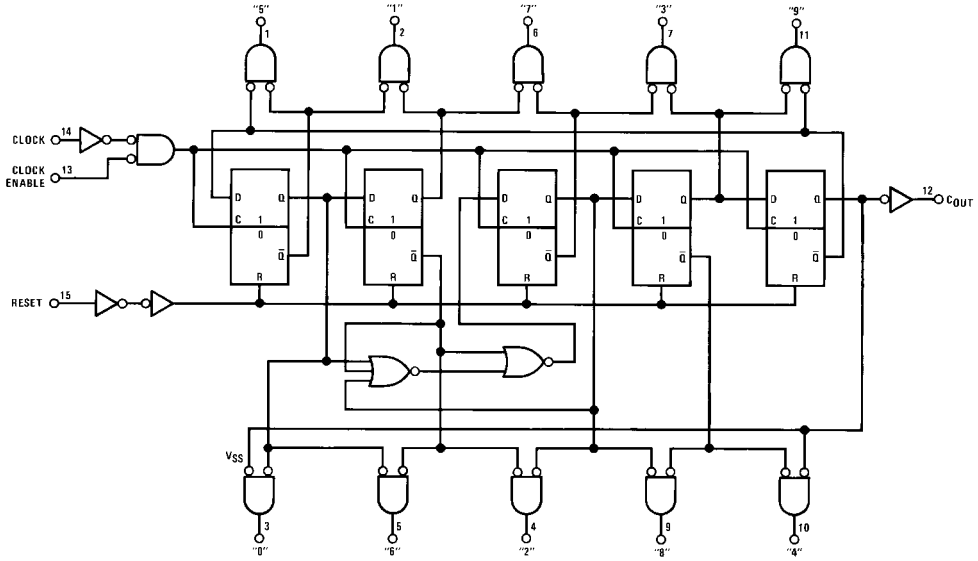
Pin Assignments for DIP and SOIC
CD4022B



Top View

Logic Diagrams

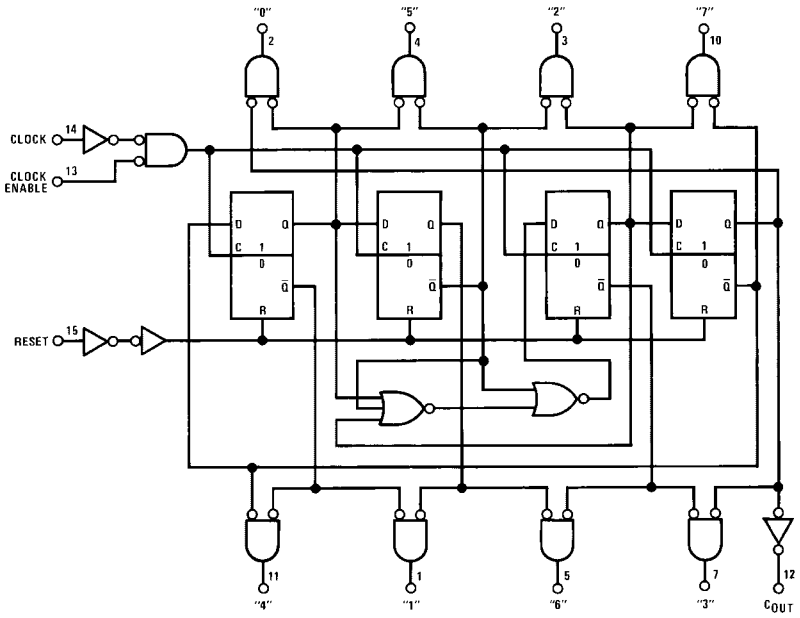
CD4017B



Terminal No. 8 = GND

Terminal No. 16 = V_{DD}

CD4022B

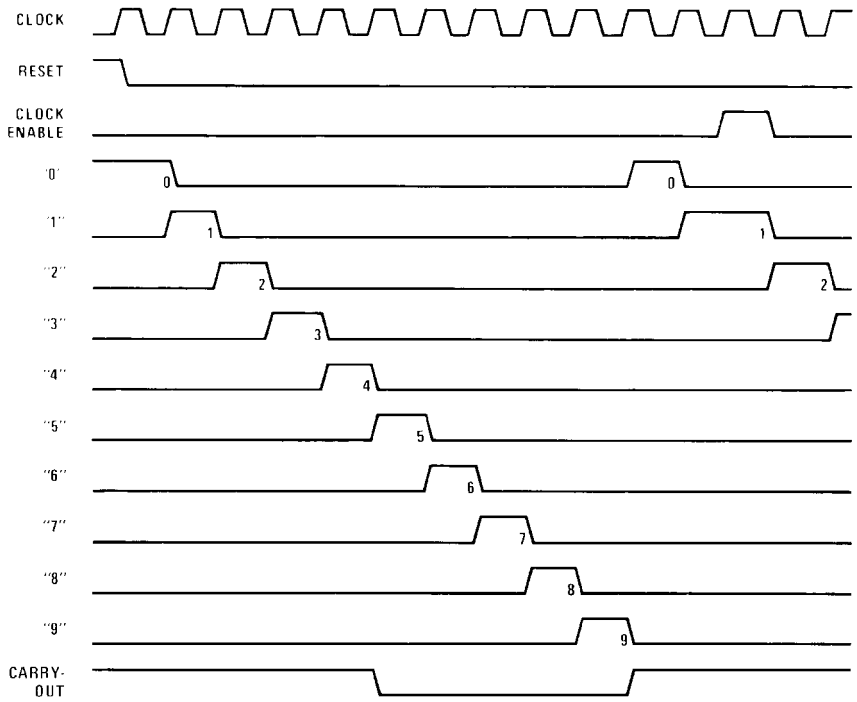


Terminal No. 16 = V_{DD}

Terminal No. 8 = GND

Timing Diagrams

CD4017B



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