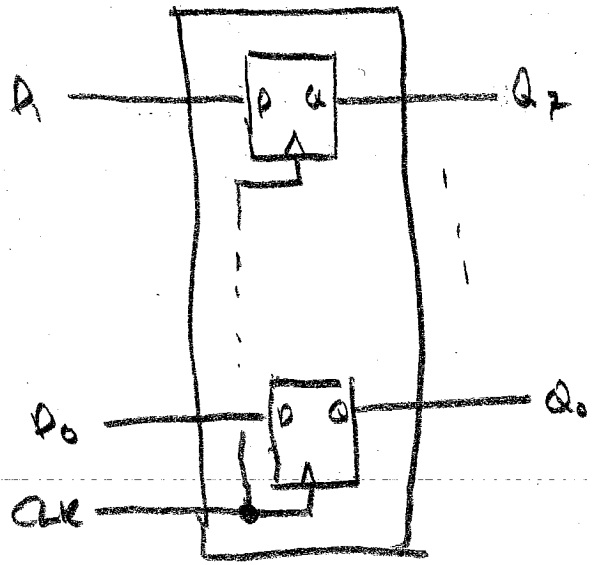
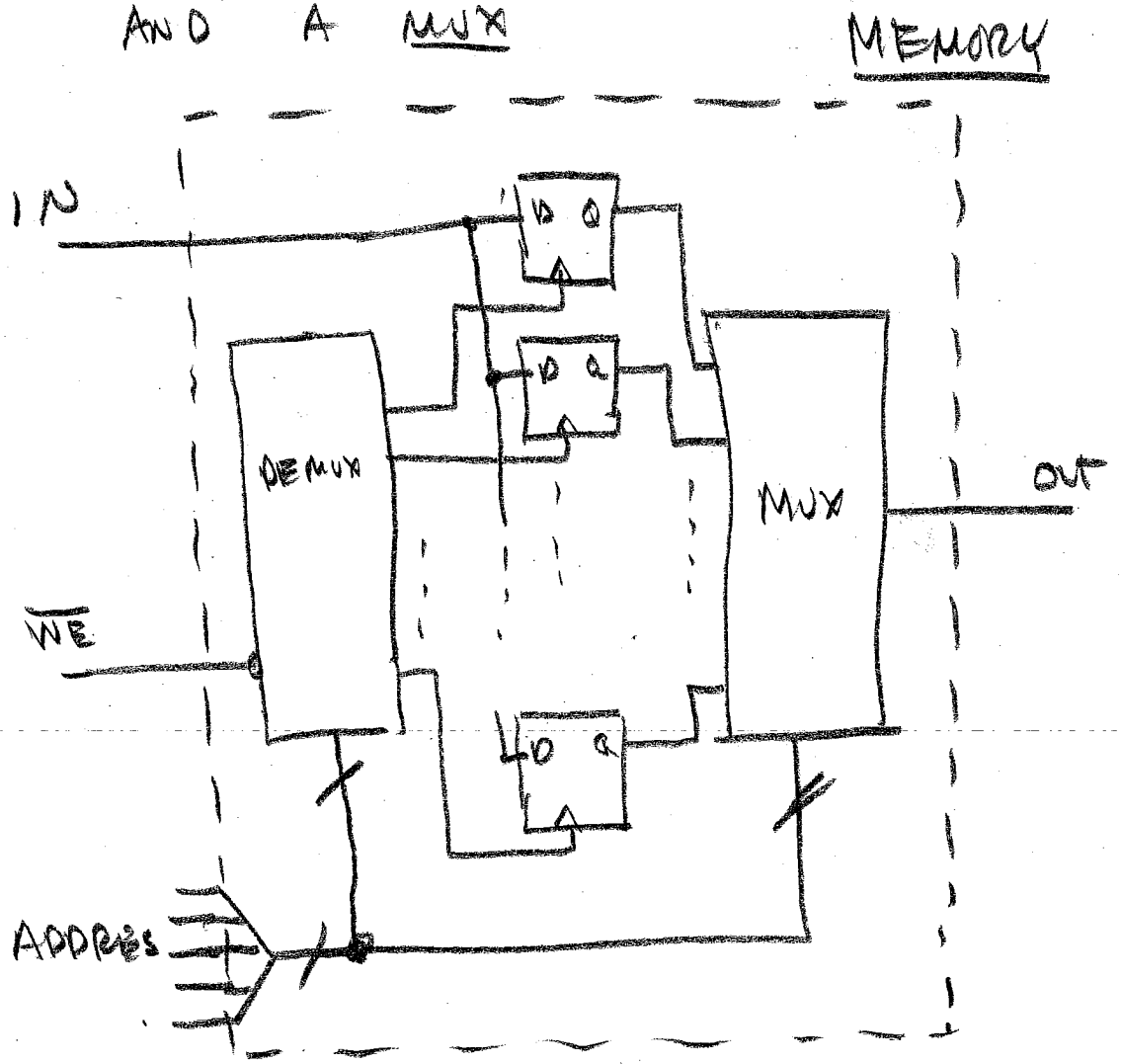
MEMORY

SIMPLEST PICTURE = LOTS OF SR LATCHES BETWEEN A DEMUX AND A MUX





JARGON – AND MEMORY TYPES

RAM – "RANDOM ACCESS MEMORY"
↳ NEED ADDRESS FOR EACH CELL

ROM – "READ-ONLY MEMORY"
↳ LIKE RAM, BUT CAN WRITE ONLY ONCE

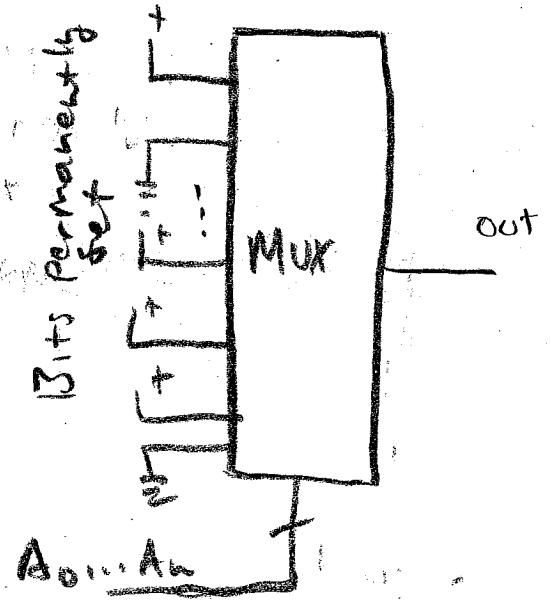
→ SRAM – "STATIC RAM" – SIMPLE WIRING & TIMING
RELATIVELY SLOW & SMALL
↳ STATE DOES NOT CHANGE
AS LONG AS POWER IS ON.

→ DRAM – "DYNAMIC RAM" – COMPLICATED WIRING
SIMPLER INTERNAL CIRCUITRY
↳ STATE MUST BE REFRESHED

→ PROM – Programmable ROM
↳ EEPROM
↳ "FLASH" MEMORY ("THUMB DRIVE")

AMONG MEMORY TYPES SRAM and old ROM IS SIMPLEST TO UNDERSTAND.

OLD ROM — JUST A BUNCH OF LINKS (FUSES) EITHER SET OR BROKEN AMONG LOGIC GATES. ONLY NEED OUTPUT:



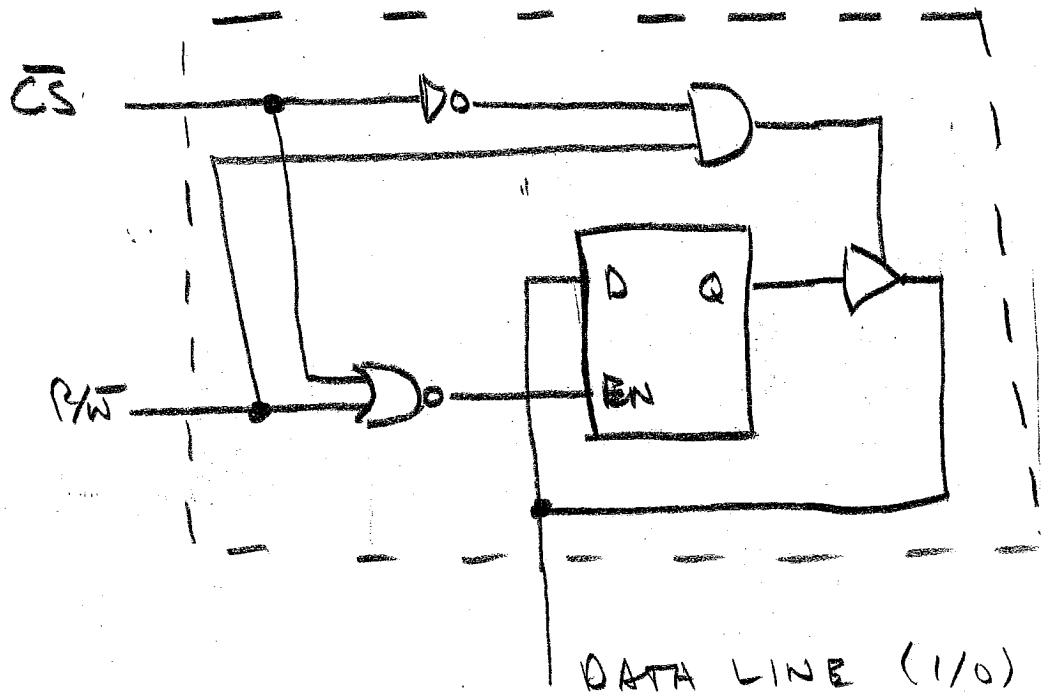
PROM ALLOWS LINKS TO BE SET BY SPECIAL EQUIPMENT.

ORIGINAL ROM HAS BITS SET BY MANUFACTURER

CHEAP TO MAKE IN LARGE QUANTITIES

"MEMORY CELL" (BAUER)

FLOP + ENABLE ("CS") + R/$\overline{W}$ + THREE-STATE OUTPUT



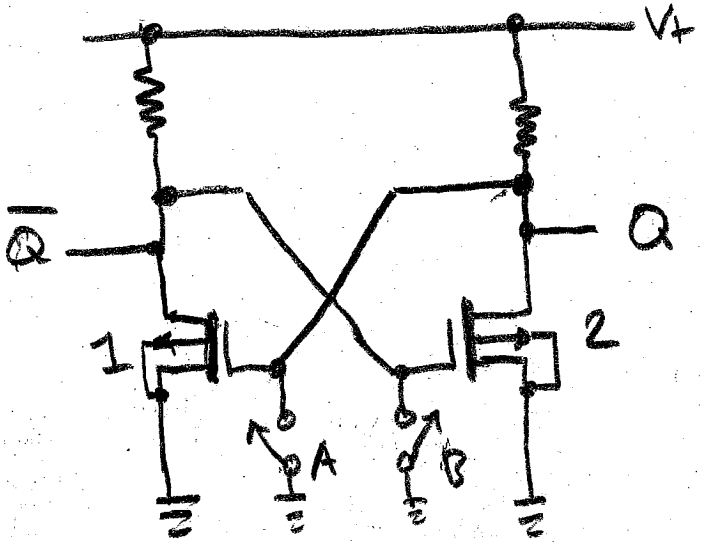
$\overline{CS}$ - HIGH
⇒ 3-STATE off
EN LOW

$\overline{CS}$ - LOW
IF R/$\overline{W}$ LOW
EN = HIGH
& 3-STATE OFF
} WRITE

$\overline{CS}$ - LOW
IF R/$\overline{W}$ HIGH
EN = LOW
& 3-STATE ON
} READ

DESIGN OF SRAM CELL

TRANSISTOR LATCH

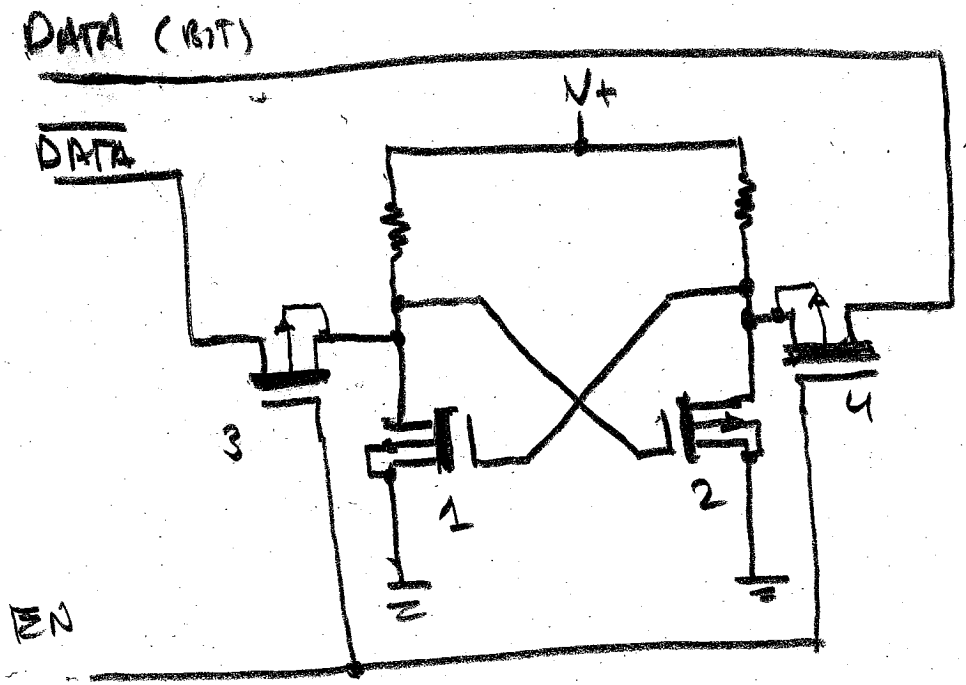


FORCE A LOW → TURN OFF 1

→ TURN ON 2 → KEEPS A LOW

→ $\overline{Q}$ = HI, Q = LOW

AFTER RELEASE



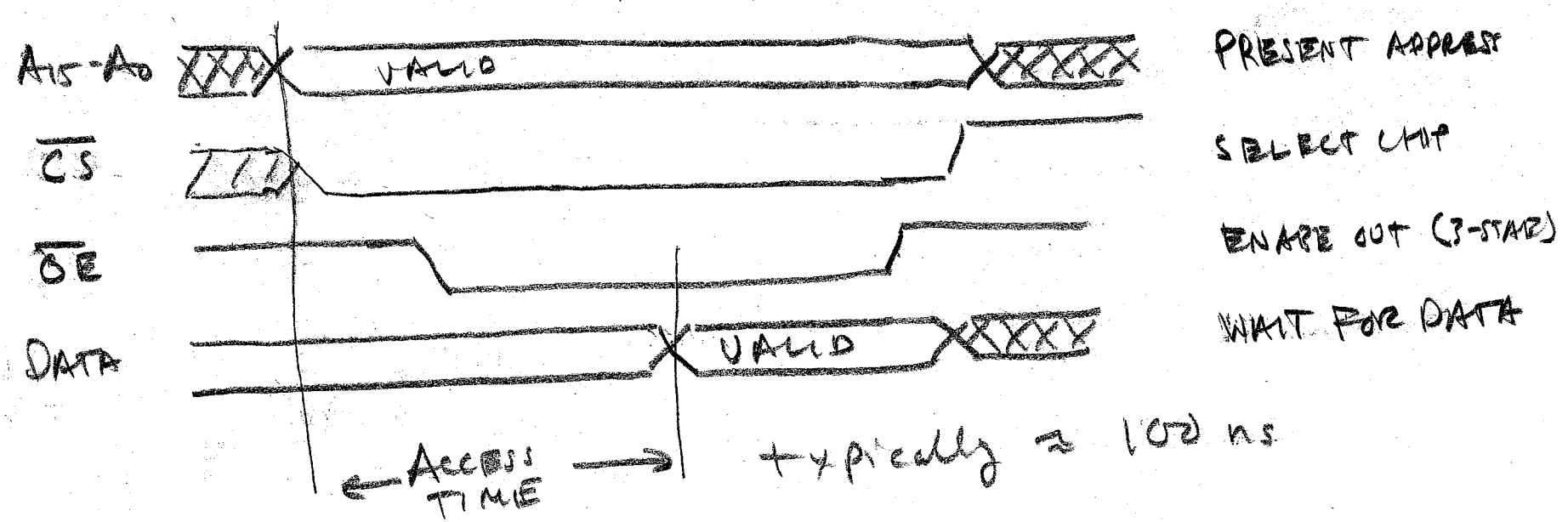
STORE – 3 & 4 OFF – LATCH HOLDS BITS

WRITE – SET DATA LINE, ENABLE 3 & 4 → FORCES NEW STATE

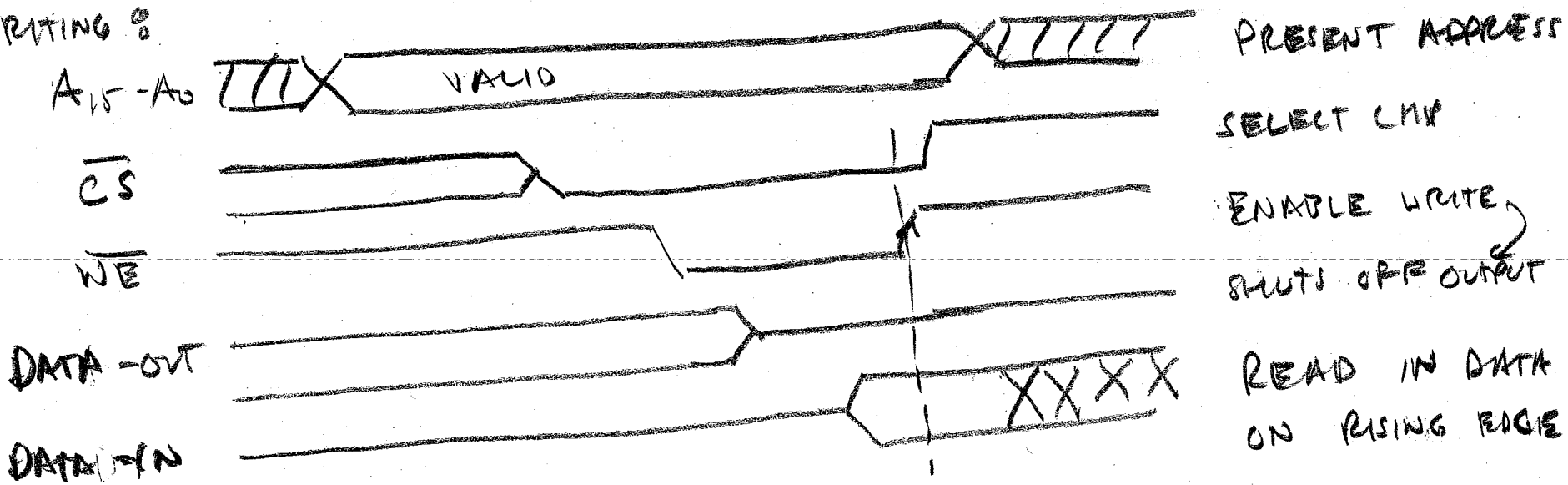
READ – (TRICKY) PUT 1's ON BOTH LINES, TURN OFF DATA LINES, ENABLE, THEN LOOK AT DATA

MEMORY TIMING (SRAM)

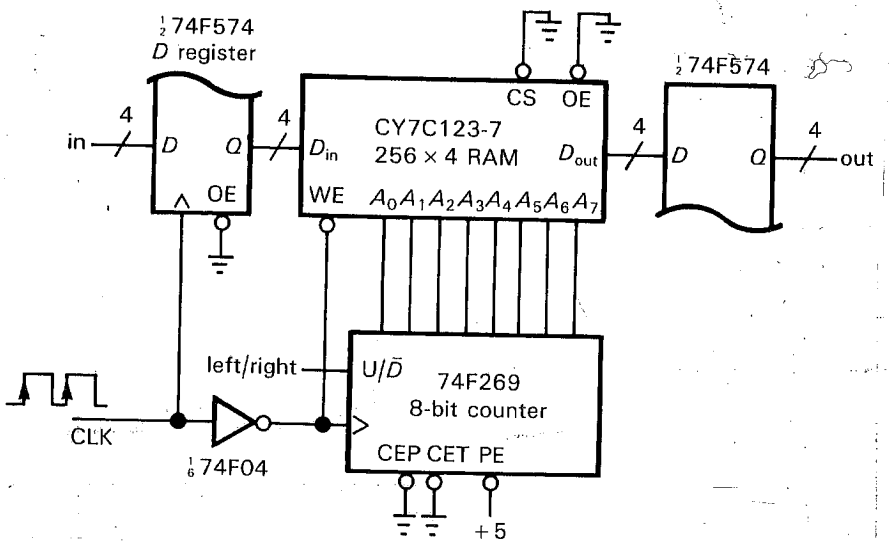
READING:



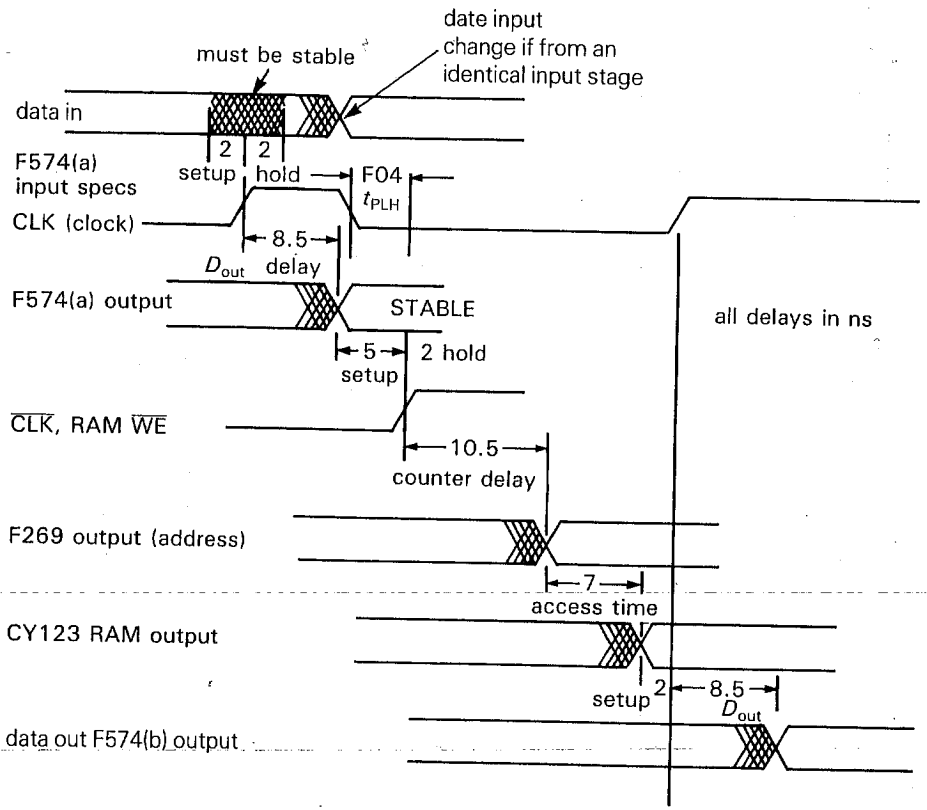
WRITING:



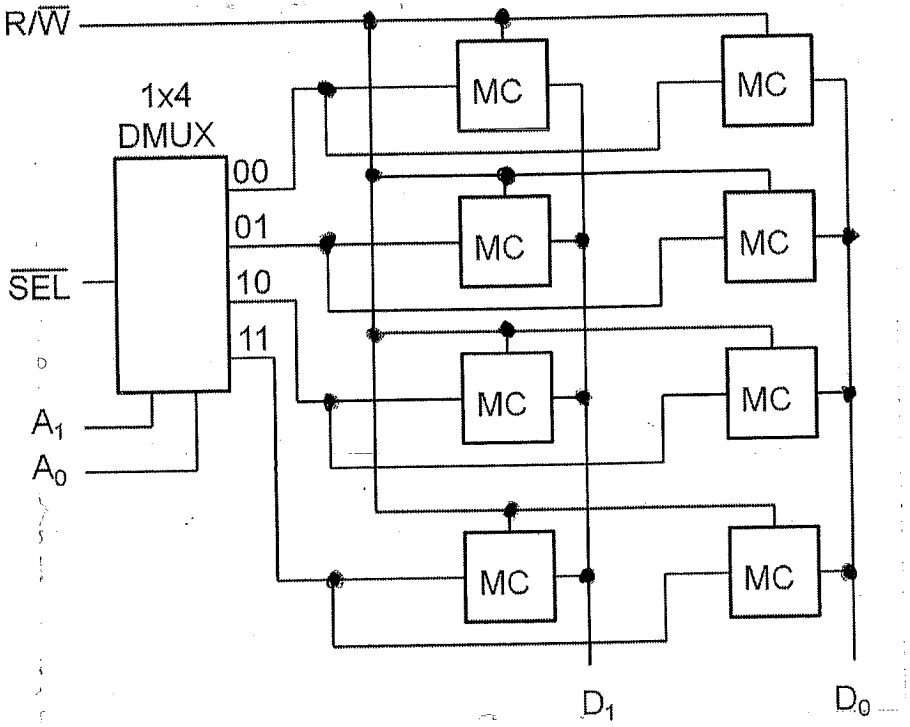
EXAMPLE — USING SRAM AS A REALLY BIG SHIFT REGISTER (H&H)



F04 t_{PLH} delay	3.7ns	
F374 D_{out} delay	8.5ns	13.5 − 3.7 = 9.8ns HI
CYC123 setup time	5	
F269 counter out delay	10.5	
CYC123 access time	7	19.5 + 3.7 = 23.2ns LO
F374 D_{IN} setup time	2	
shift clock period(min)	33 ns	



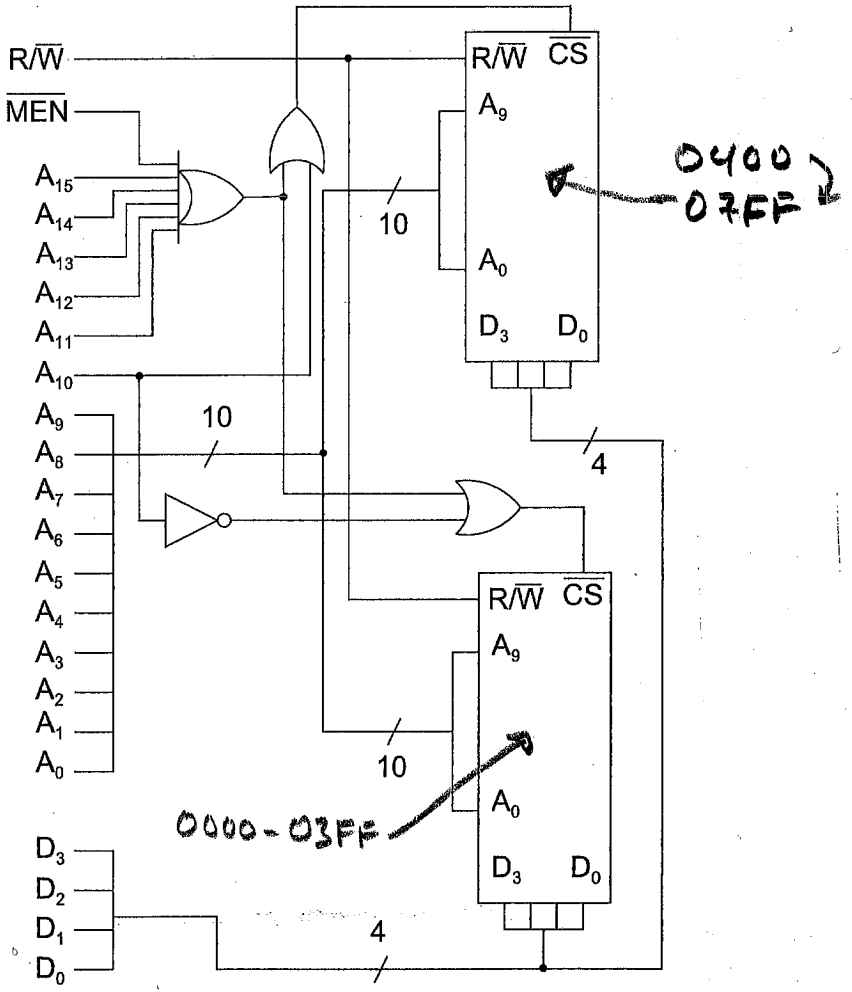
MEMORY ORGANIZATION & ADDRESSING



MEMORY SPECIFIED BY
(ADDRESSES) x (BITS)

HERE $A_0 - A_9$ = 10 BIT ADDRESS = 2^{10} = 1024

& 4 BITS → 1024 x 4



TYPICAL WIRING FOR MEMORY CHIPS

1024 WORD x 4 BIT STATIC RAM

TMM2114AP-12
TMM2114AP-15

DESCRIPTION

The TMM2114AP is a 4,096 bits static random access memory organized as 1024 words by 4 bits and operates from a single 5V power supply. Toshiba's high performance device technology provides both high speed and low power features with maximum operating current of 60mA and maximum access time of 120ns/150ns. The memories with 6Tr. cells are fully static in operation and require no clocks or refresh periods. Therefore the TMM2114AP is most suitable for use in microcomputer peripheral memory where high performance, lower cost, simple interfacing are required.

The TMM2114AP is fabricated with N channel silicon gate depletion load type MOS technology by ion implantation for high speed, high performance and high reliability.

The chip is moulded in the standard 18 pin plastic package with 0.3 inch width.

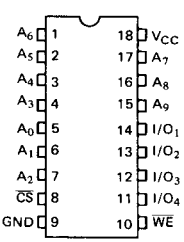
FEATURES

- 1024 Word x 4 Bit organization
- Fully static operation
- Single 5V supply voltage
- All inputs and outputs: Directly TTL compatible
- Three state output: Wired OR capability
- Common data inputs and outputs
- 2114A type pin compatible
- Fast Access time and Low Operating Current (Max.)

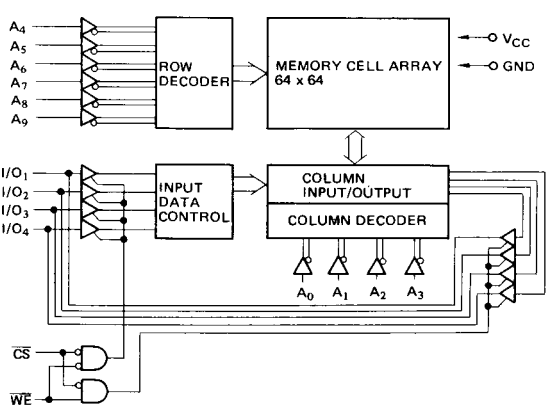
	TMM2114AP-12	TMM2114AP-15
$t_{ACC(ns)}$	120	150
$I_{CC(mA)}$	60	60

- Input protected: All inputs have protection against static charge.

PIN CONNECTION (TOP VIEW)



BLOCK DIAGRAM



PIN NAMES

$A_0 \sim A_3$	Column Address Inputs
$A_4 \sim A_9$	Row Address Inputs
$I/O_1 \sim I/O_4$	Data Input/Output
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
V_{CC}	Supply Voltage
GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	MODE
H	*	*	High Impedance	Non-decode
L	H	*	Data Output	Read
L	L	H/L	Data Input	Write

* L or H

MAXIMUM RATINGS

SYMBOL	ITEM	RATING	UNIT
V_{CC}	Supply Voltage	−0.5 ~ 7.0	V
$V_{I/O}$	Input/Output Voltage	−0.5 ~ 7.0	V
T_{OPR}	Operating Temperature	0 ~ 70	°C
T_{STG}	Storage Temperature	−55 ~ 150	°C
T_{SOLDER}	Soldering Temperature · Time	260 · 10	°C · sec
P_D	Power Dissipation (Ta = 70°C)	850	mW

DC RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{IH}	Input High Voltage	2.0	–	V_{CC}+1.0	V
V_{IL}	Input Low Voltage	−0.5	–	0.8	V
V_{CC}	Supply Voltage	4.5	5	5.5	V

DC CHARACTERISTICS (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.*	MAX.	UNIT
I_{IL}	Input Leakage Current	V_{IN} = 0V ~ 5.5V	−10	–	10	μA
V_{OH}	Output High Voltage	I_{SOURCE} = −1.0mA	2.4	–	–	V
V_{OL}	Output Low Voltage	I_{SINK} = 2.1mA	–	–	0.4	V
I_{LO}	Output Leakage Current	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} V_{OUT} = 0.0V ~ 5.5V	−10	–	10	μA
I_{CC}	Supply Current	I_{OUT} = 0mA	–	–	60	mA

* Ta = 25°C, V_{CC} = 5V

AC CHARACTERISTICS (Ta = 0 ~ 70°C, V_{CC} = 5V ± 10%, 1-TTL Gate & C_L = 100pF, t_r, t_f ≦ 10 ns)

READ CYCLE

SYMBOL	PARAMETER	TMM2114AP-12			TMM2114AP-15			UNIT
		MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
t_{RC}	Read Cycle Time	120	–	–	150	–	–	ns
t_{ACC}	Access Time	–	–	120	–	–	150	ns
t_{CO}	Chip Select Time	–	–	70	–	–	70	ns
t_{CX}	Output Active from $\overline{CS}$	10	–	–	10	–	–	ns
t_{OD}	Deselect Time	0	–	35	0	–	40	ns
t_{OH}	Output Hold From Address Change	20	–	–	20	–	–	ns

* Ta = 25°C, V_{CC} = 5V

WRITE CYCLE

SYMBOL	PARAMETER	TMM2114AP-12			TMM2114AP-15			UNIT
		MIN.	TYP.*	MAX.	MIN.	TYP.*	MAX.	
t_{WC}	Write Cycle Time	120	–	–	150	–	–	ns
t_{WP}	Write Pulse Width	70	–	–	90	–	–	ns
t_{WR}	Write Recovery Time	0	–	–	0	–	–	ns
t_{ODW}	Output High Z From $\overline{WE}$	0	–	35	0	–	40	ns
t_{DS}	Data Setup Time	70	–	–	90	–	–	ns
t_{DH}	Data Hold Time	0	–	–	0	–	–	ns
t_{AW}	Address to Write Setup Time	0	–	–	0	–	–	ns

* Ta = 25°C, V_{CC} = 5V

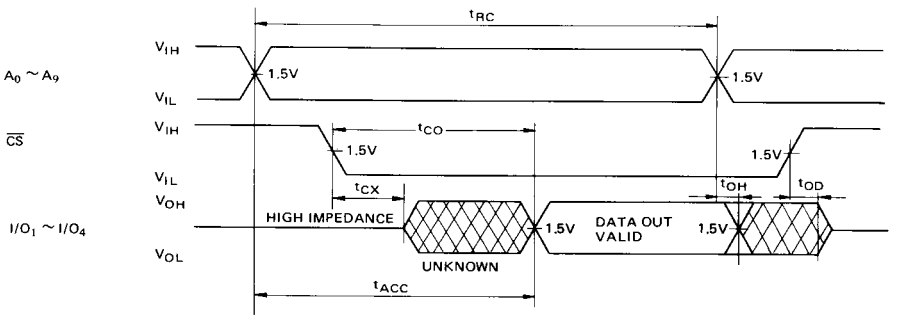
CAPACITANCE (Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN} = AC Ground	–	–	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = AC Ground	–	–	10	pF

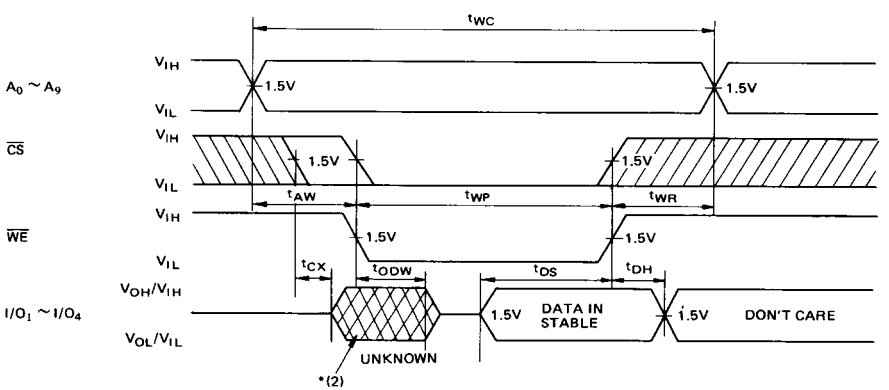
Note: This parameter is periodically sampled and not 100% tested.

TIMING WAVEFORMS

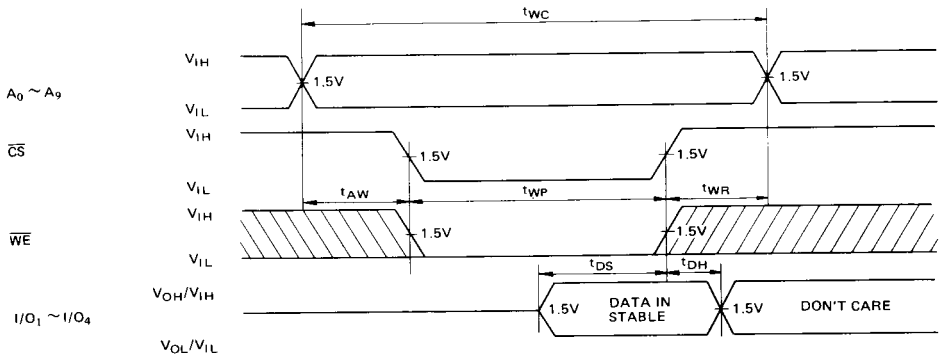
- **READ CYCLE**



- **WRITE CYCLE [1] *(1)**



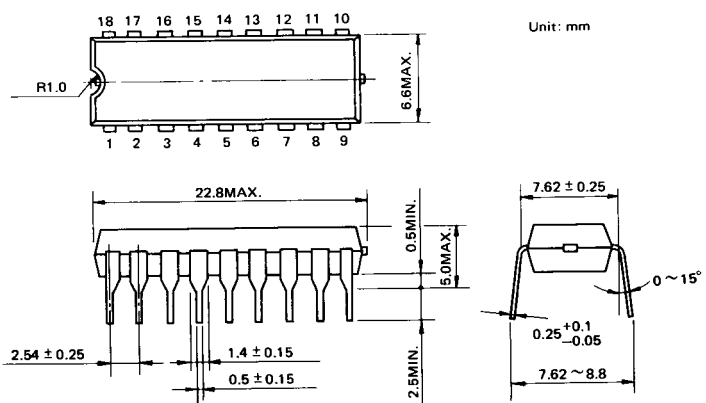
- **WRITE CYCLE [2] *(1)**



Note *(1): A write occurs during the overlap of a low $\overline{CS}$ and low $\overline{WE}$.
And twp is specified as the logical 'AND' of $\overline{CS}$ and $\overline{WE}$.

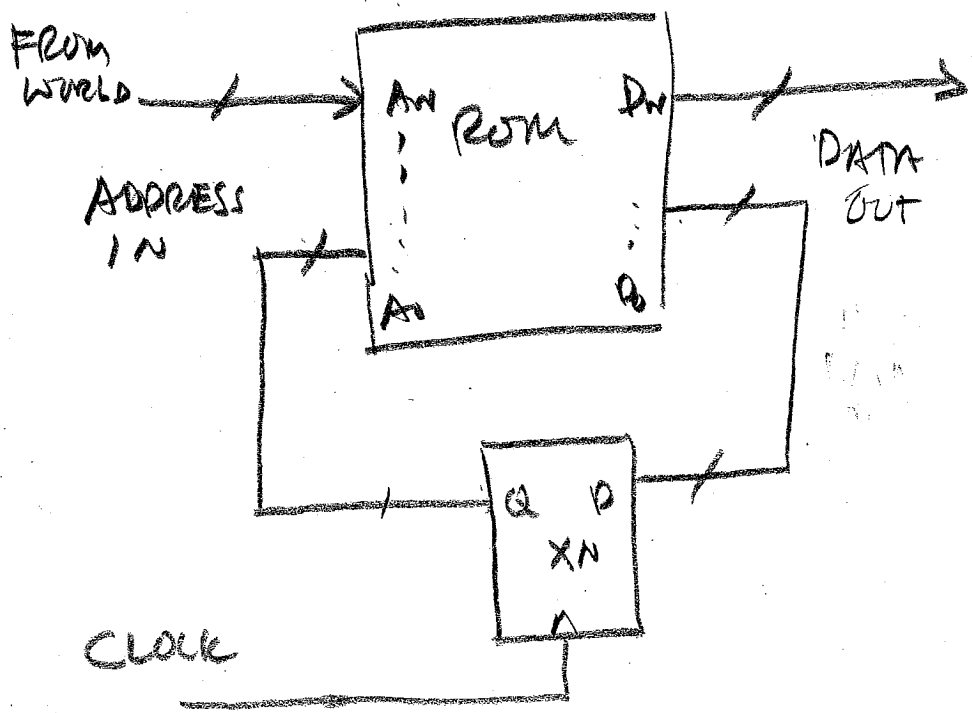
*(2): If the $\overline{CS}$ low transition occurs simultaneously with or latter from $\overline{WE}$ low transition, the output buffers remain in a high impedance state in this period.

OUTLINE DRAWINGS



Note: All dimensions are in millimeters. Each lead pitch is 2.54mm.
All leads are located within 0.25mm of their true longitudinal position with respect to No. 1 and No. 18 leads.

CAN USE MEMORY AS "LOGIC" IN A STATE MACHINE (ROM)



EXAMPLE: FIBONACCI COUNTER

$A_2 A_1 A_0$	$D_4 D_3$	$D_2 D_1 D_0$
0 0 0	0 0	0 0 1
0 0 1	0 1	0 1 0
0 1 0	0 1	0 1 1
0 1 1	1 0	1 0 0
1 0 0	1 1	0 0 0

↑ SETS NEXT ADDRESS

↑ OUT TO WORLD

A BRIEF LOOK AT NEXT WEEK'S LAB

COUNTERS

YOU WILL BUILD & STUDY

- A BCD COUNTER (LS90)
- A HEX COUNTER (LS93)
- A "STOPWATCH" USING 2 LS90s

MOTOROLA

SN54/74LS90
SN54/74LS92
SN54/74LS93

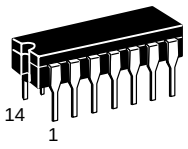
DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER

DECADE COUNTER;
DIVIDE-BY-TWELVE COUNTER;
4-BIT BINARY COUNTER

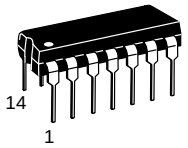
LOW POWER SCHOTTKY

The SN54/74LS90, SN54/74LS92 and SN54/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggered by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

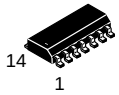
- Low Power Consumption . . . Typically 45 mW
- High Count Rates . . . Typically 42 MHz
- Choice of Counting Modes . . . BCD, Bi-Quinary, Divide-by-Twelve, Binary
- Input Clamp Diodes Limit High Speed Termination Effects



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

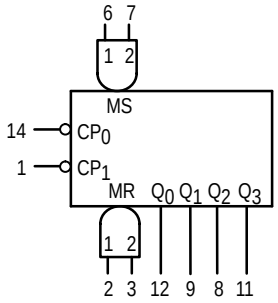
SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

PIN NAMES		**LOADING** (Note a)	
		HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 Section	0.5 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 Section (LS90), ÷6 Section (LS92)	0.5 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷8 Section (LS93)	0.5 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, LS90) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5 (2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 (LS90), ÷6 (LS92), ÷8 (LS93) Sections (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military, (54) and 5 U.L. for commercial (74) Temperature Ranges.
c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ input of the device.
d. To insure proper operation the rise (t_r) and fall time (t_f) of the clock must be less than 100 ns.

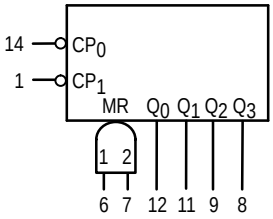
LOGIC SYMBOL

LS90



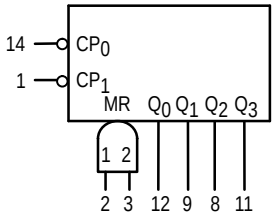
V_{CC} = PIN 5
GND = PIN 10
NC = PINS 4, 13

LS92



V_{CC} = PIN 5
GND = PIN 10
NC = PINS 2, 3, 4, 13

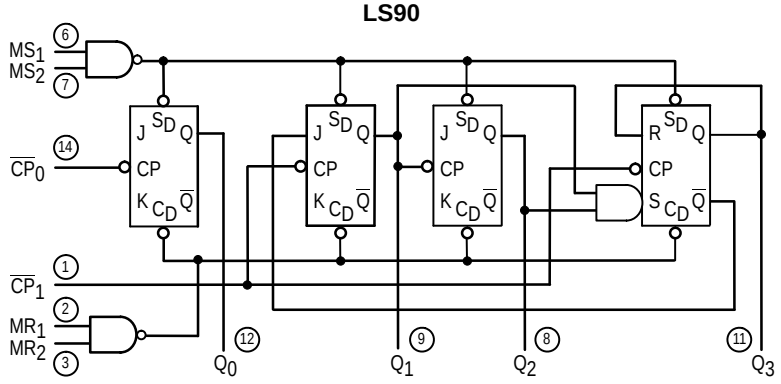
LS93



V_{CC} = PIN 5
GND = PIN 10
NC = PIN 4, 6, 7, 13

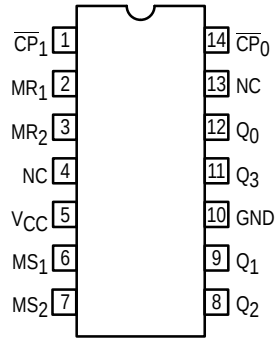
LOGIC DIAGRAM

LS90



○ = PIN NUMBERS
V_{CC} = PIN 5
GND = PIN 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

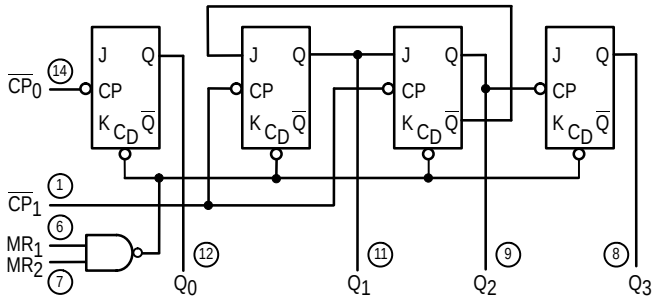


NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

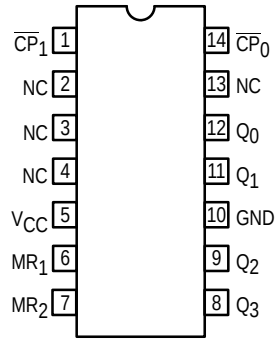
LOGIC DIAGRAM

LS92



○ = PIN NUMBERS
V_{CC} = PIN 5
GND = PIN 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

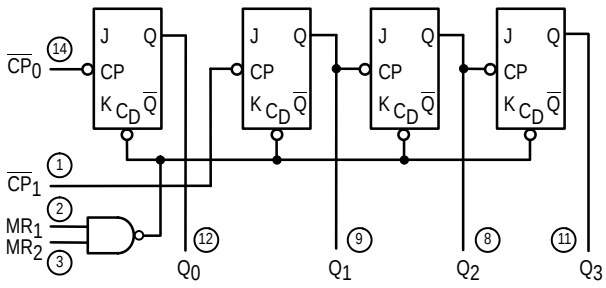


NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

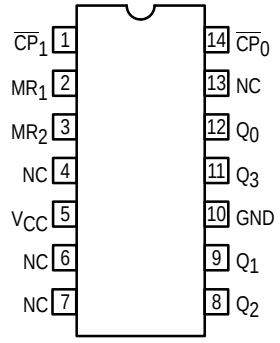
LOGIC DIAGRAM

LS93



○ = PIN NUMBERS
V_{CC} = PIN 5
GND = PIN 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = NO INTERNAL CONNECTION

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

FUNCTIONAL DESCRIPTION

The LS90, LS92, and LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide-by-six (LS92), or divide-by-eight (LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \bullet MR_2$) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \bullet MS_2$) is provided on the LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

LS90

A. BCD Decade (8421) Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

LS92

A. Modulo 12, Divide-By-Twelve Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and Q_3 produces a symmetrical divide-by-twelve square wave output.

B. Divide-By-Two and Divide-By-Six Counter —No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

LS93

A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter— The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS90
MODE SELECTION

RESET / SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS92 AND LS93
MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS90
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to Input CP_1 for BCD count.

LS92
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

NOTE: Output Q_0 is connected to Input CP_1.

LS93
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

NOTE: Output Q_0 is connected to Input CP_1.

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	–55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			–0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			–0.65	–1.5	V	V_{CC} = MIN, I_{IN} = –18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	µA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current $\overline{MS}$, $\overline{MR}$ $\overline{CP}_0$ $\overline{CP}_1$ (LS90, LS92) $\overline{CP}_1$ (LS93)				–0.4 –2.4 –3.2 –1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		–20		–100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				15	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C, V_{CC} = 5.0 V, C_L = 15 pF)

Symbol	Parameter	Limits									Unit
		LS90			LS92			LS93			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	$\overline{CP}_0$ Input Clock Frequency	32			32			32			MHz
f_{MAX}	$\overline{CP}_1$ Input Clock Frequency	16			16			16			MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		10 12	16 18		10 12	16 18		10 12	16 18	ns
t_{PLH} t_{PHL}	$\overline{CP}_0$ Input to Q_3 Output		32 34	48 50		32 34	48 50		46 46	70 70	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_1 Output		10 14	16 21		10 14	16 21		10 14	16 21	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_2 Output		21 23	32 35		10 14	16 21		21 23	32 35	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_3 Output		21 23	32 35		21 23	32 35		34 34	51 51	ns
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		20	30							ns
t_{PHL}	MS Input to Q_1 and Q_2 Outputs		26	40							ns
t_{PHL}	MR Input to Any Output		26	40		26	40		26	40	ns

AC SETUP REQUIREMENTS (T_A = 25°C, V_{CC} = 5.0 V)

Symbol	Parameter	Limits						Unit
		LS90		LS92		LS93		
		Min	Max	Min	Max	Min	Max	
t_W	$\overline{CP}_0$ Pulse Width	15		15		15		ns
t_W	$\overline{CP}_1$ Pulse Width	30		30		30		ns
t_W	MS Pulse Width	15						ns
t_W	MR Pulse Width	15		15		15		ns
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		25		ns

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs

AC WAVEFORMS

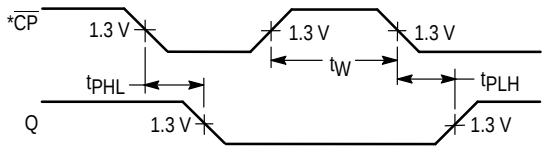


Figure 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

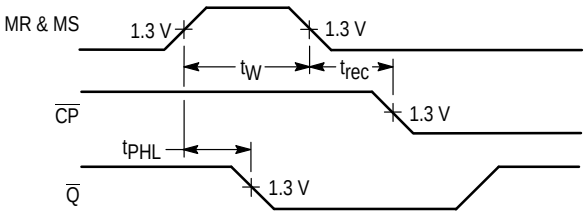


Figure 2

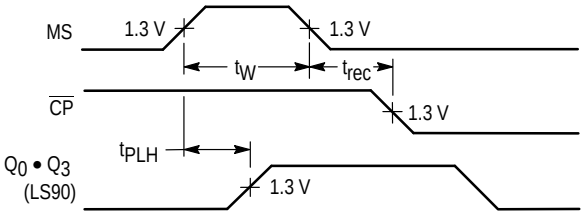


Figure 3

MOTOROLA

BCD DECADE COUNTERS/ 4-BIT BINARY COUNTERS

SN54/74LS160A
SN54/74LS161A
SN54/74LS162A
SN54/74LS163A

BCD DECADE COUNTERS/ 4-BIT BINARY COUNTERS

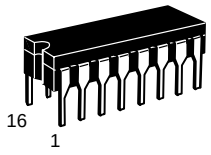
LOW POWER SCHOTTKY

The LS160A/161A/162A/163A are high-speed 4-bit synchronous counters. They are edge-triggered, synchronously presettable, and cascadable MSI building blocks for counting, memory addressing, frequency division and other applications. The LS160A and LS162A count modulo 10 (BCD). The LS161A and LS163A count modulo 16 (binary.)

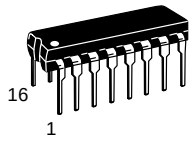
The LS160A and LS161A have an asynchronous Master Reset (Clear) input that overrides, and is independent of, the clock and all other control inputs. The LS162A and LS163A have a Synchronous Reset (Clear) input that overrides all other control inputs, but is active only during the rising clock edge.

	BCD (Modulo 10)	Binary (Modulo 16)
Asynchronous Reset	LS160A	LS161A
Synchronous Reset	LS162A	LS163A

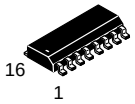
- Synchronous Counting and Loading
- Two Count Enable Inputs for High Speed Synchronous Expansion
- Terminal Count Fully Decoded
- Edge-Triggered Operation
- Typical Count Rate of 35 MHz
- ESD > 3500 Volts


16
1

J SUFFIX
CERAMIC
CASE 620-09


16
1

N SUFFIX
PLASTIC
CASE 648-08

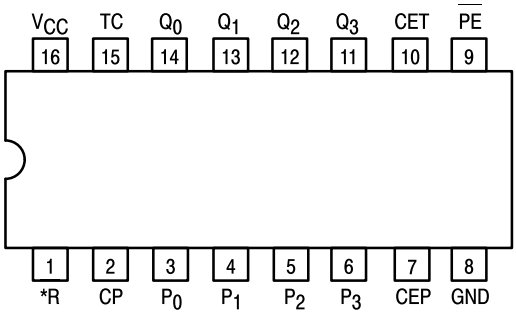

16
1

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

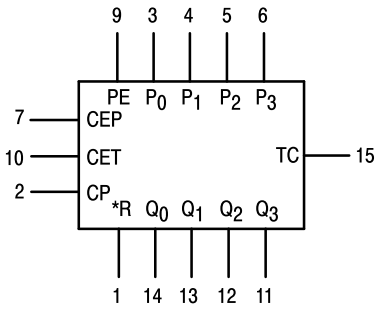
*MR for LS160A and LS161A
*SR for LS162A and LS163A

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{PE}$	Parallel Enable (Active LOW) Input	1.0 U.L.	0.5 U.L.
P_0-P_3	Parallel Inputs	0.5 U.L.	0.25 U.L.
CEP	Count Enable Parallel Input	0.5 U.L.	0.25 U.L.
CET	Count Enable Trickle Input	1.0 U.L.	0.5 U.L.
CP	Clock (Active HIGH Going Edge) Input	0.5 U.L.	0.25 U.L.
$\overline{MR}$	Master Reset (Active LOW) Input	0.5 U.L.	0.25 U.L.
SR	Synchronous Reset (Active LOW) Input	1.0 U.L.	0.5 U.L.
Q_0-Q_3	Parallel Outputs (Note b)	10 U.L.	5 (2.5) U.L.
TC	Terminal Count Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

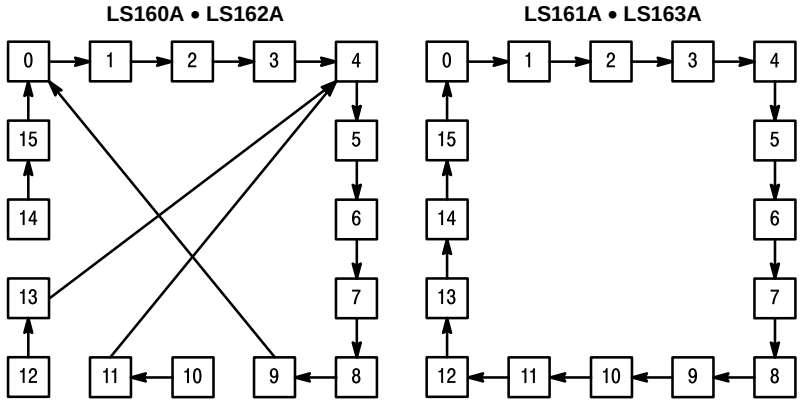
LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

*MR for LS160A and LS161A
*SR for LS162A and LS163A

STATE DIAGRAM



LOGIC EQUATIONS

Count Enable = CEP • CET • PE

TC for LS160A & LS162A = CET • Q_0 • Q_1 • Q_2 • Q_3

TC for LS161A & LS163A = CET • Q_0 • Q_1 • Q_2 • Q_3

Preset = PE • CP + (rising clock edge)

Reset = MR (LS160A & LS161A)

Reset = SR • CP + (rising clock edge)
(LS162A & LS163A)

NOTE:
The LS160A and LS162A can be preset to any state, but will not count beyond 9. If preset to state 10, 11, 12, 13, 14, or 15, it will return to its normal sequence within two clock pulses.

FUNCTIONAL DESCRIPTION

The LS160A/161A/162A/163A are 4-bit synchronous counters with a synchronous Parallel Enable (Load) feature. The counters consist of four edge-triggered D flip-flops with the appropriate data routing networks feeding the D inputs. All changes of the Q outputs (except due to the asynchronous Master Reset in the LS160A and LS161A) occur as a result of, and synchronous with, the LOW to HIGH transition of the Clock input (CP). As long as the set-up time requirements are met, there are no special timing or activity constraints on any of the mode control or data inputs.

Three control inputs — Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) — select the mode of operation as shown in the tables below. The Count Mode is enabled when the CEP, CET, and PE inputs are HIGH. When the PE is LOW, the counters will synchronously load the data from the parallel inputs into the flip-flops on the LOW to HIGH transition of the clock. Either the CEP or CET can be used to inhibit the count sequence. With the PE held HIGH, a LOW on either the CEP or CET inputs at least one set-up time prior to the LOW to HIGH clock transition will cause the existing output states to be retained. The AND feature of the two Count Enable inputs (CET • CEP) allows synchronous cascading without external gating and without delay accumulation over any practical number of bits or digits.

The Terminal Count (TC) output is HIGH when the Count Enable Trickle (CET) input is HIGH while the counter is in its maximum count state (HLLH for the BCD counters, HHHH for the Binary counters). Note that TC is fully decoded and will, therefore, be HIGH only for one count state.

The LS160A and LS162A count modulo 10 following a binary coded decimal (BCD) sequence. They generate a TC output when the CET input is HIGH while the counter is in state 9 (HLLH). From this state they increment to state 0 (LLLL). If loaded with a code in excess of 9 they return to their legitimate sequence within two counts, as explained in the state diagram. States 10 through 15 do *not* generate a TC output.

The LS161A and LS163A count modulo 16 following a binary sequence. They generate a TC when the CET input is HIGH while the counter is in state 15 (HHHH). From this state they increment to state 0 (LLLL).

The Master Reset ($\overline{MR}$) of the LS160A and LS161A is asynchronous. When the MR is LOW, it overrides all other input conditions and sets the outputs LOW. The MR pin should never be left open. If not used, the MR pin should be tied through a resistor to V_{CC}, or to a gate output which is permanently set to a HIGH logic level.

The active LOW Synchronous Reset ($\overline{SR}$) input of the LS162A and LS163A acts as an edge-triggered control input, overriding CET, CEP and PE, and resetting the four counter flip-flops on the LOW to HIGH transition of the clock. This simplifies the design from race-free logic controlled reset circuits, e.g., to reset the counter synchronously after reaching a predetermined value.

MODE SELECT TABLE

*SR	PE	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	RESET (Clear)
H	L	X	X	LOAD (P_n Q_n)
H	H	H	H	COUNT (Increment)
H	H	L	X	NO CHANGE (Hold)
H	H	X	L	NO CHANGE (Hold)

*For the LS162A and LS163A only.

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

LS160A and LS161A
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Limits Typ	Limits Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current MR, Data, CEP, Clock PE, CET				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	MR, Data, CEP, Clock PE, CET				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current MR, Data, CEP, Clock PE, CET				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				31 32	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

LS162A and LS163A
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current Data, CEP, Clock PE, CET, SR				20 40	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
	Data, CEP, Clock PE, CET, SR				0.1 0.2	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current Data, CEP, Clock, PE, $\overline{SR}$ CET				−0.4 −0.8	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH Total, Output LOW				31 32	mA	V_{CC} = MAX	

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
f_{MAX}	Maximum Clock Frequency	25	32		MHz	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay Clock to TC		20 18	35 35	ns	
t_{PLH} t_{PHL}	Propagation Delay Clock to Q		13 18	24 27	ns	
t_{PLH} t_{PHL}	Propagation Delay CET to TC		9.0 9.0	14 14	ns	
t_{PHL}	$\overline{MR}$ or $\overline{SR}$ to Q		20	28	ns	

AC SETUP REQUIREMENTS (T_A = 25°C)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t_WCP	Clock Pulse Width Low	25			ns	V_{CC} = 5.0 V
t_W	MR or SR Pulse Width	20			ns	
t_s	Setup Time, other*	20			ns	
t_s	Setup Time PE or SR	25			ns	
t_h	Hold Time, data	3			ns	
t_h	Hold Time, other	0			ns	
t_{rec}	Recovery Time MR to CP	15			ns	

*CEP, CET or DATA

DEFINITION OF TERMS

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.

RECOVERY TIME (t_{rec}) — is defined as the minimum time required between the end of the reset pulse and the clock transition from LOW to HIGH in order to recognize and transfer HIGH Data to the Q outputs.

AC WAVEFORMS

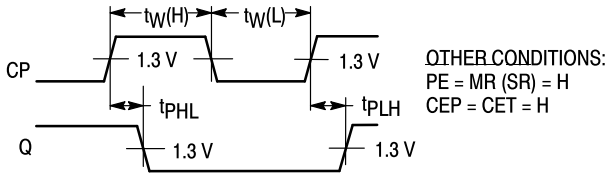


Figure 1. Clock to Output Delays, Count Frequency, and Clock Pulse Width

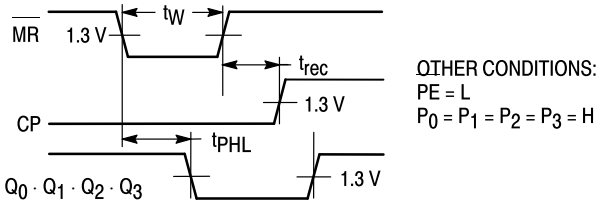


Figure 2. Master Reset to Output Delay, Master Reset Pulse Width, and Master Reset Recovery Time

AC WAVEFORMS (continued)

COUNT ENABLE TRICKLE INPUT TO TERMINAL COUNT OUTPUT DELAYS

The positive TC pulse occurs when the outputs are in the (Q_0 • Q_1 • Q_2 • Q_3) state for the LS160 and LS162 and the (Q_0 • Q_1 • Q_2 • Q_3) state for the LS161 and LS163.

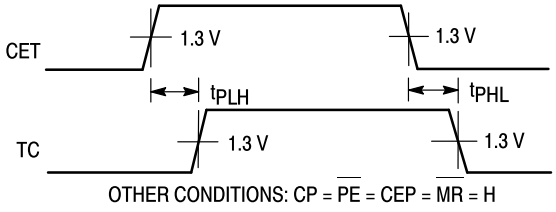


Figure 3

CLOCK TO TERMINAL COUNT DELAYS

The positive TC pulse is coincident with the output state (Q_0 • Q_1 • Q_2 • Q_3) state for the LS161 and LS163 and (Q_0 • Q_1 • Q_2 • Q_3) for the LS161 and LS163.

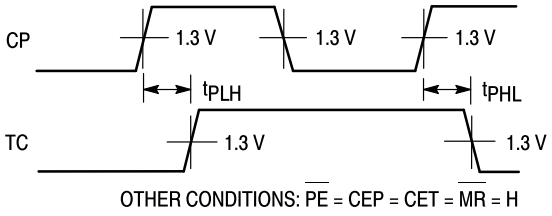


Figure 4

SETUP TIME (t_s) AND HOLD TIME (t_h) FOR PARALLEL DATA INPUTS

The shaded areas indicate when the input is permitted to change for predictable output performance.

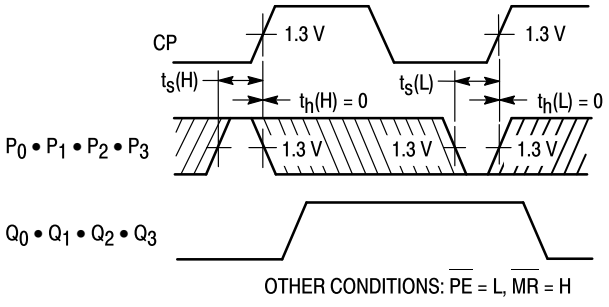


Figure 5

SETUP TIME (t_s) AND HOLD TIME (t_h) FOR COUNT ENABLE (CEP) AND (CET) AND PARALLEL ENABLE (PE) INPUTS

The shaded areas indicate when the input is permitted to change for predictable output performance.

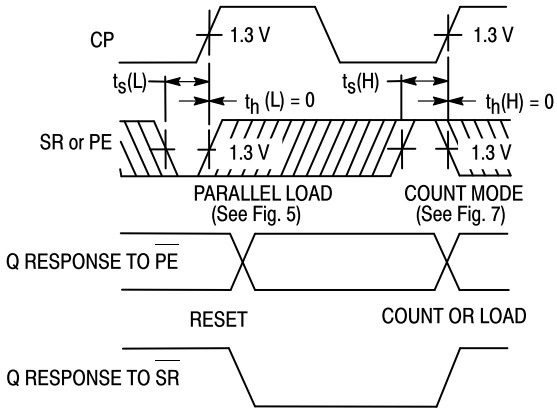


Figure 6

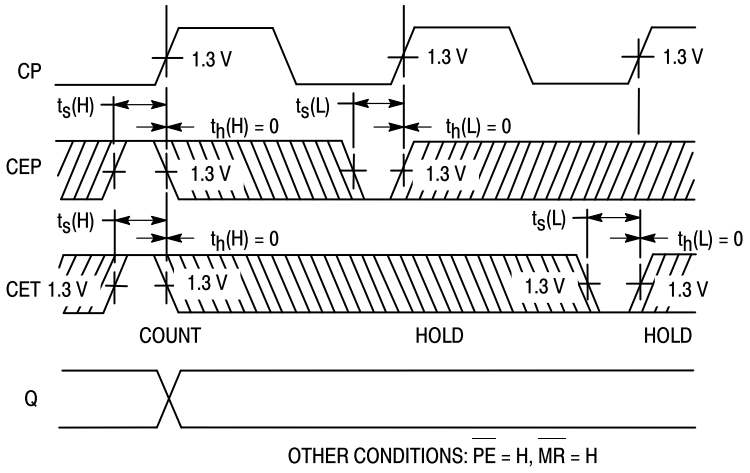
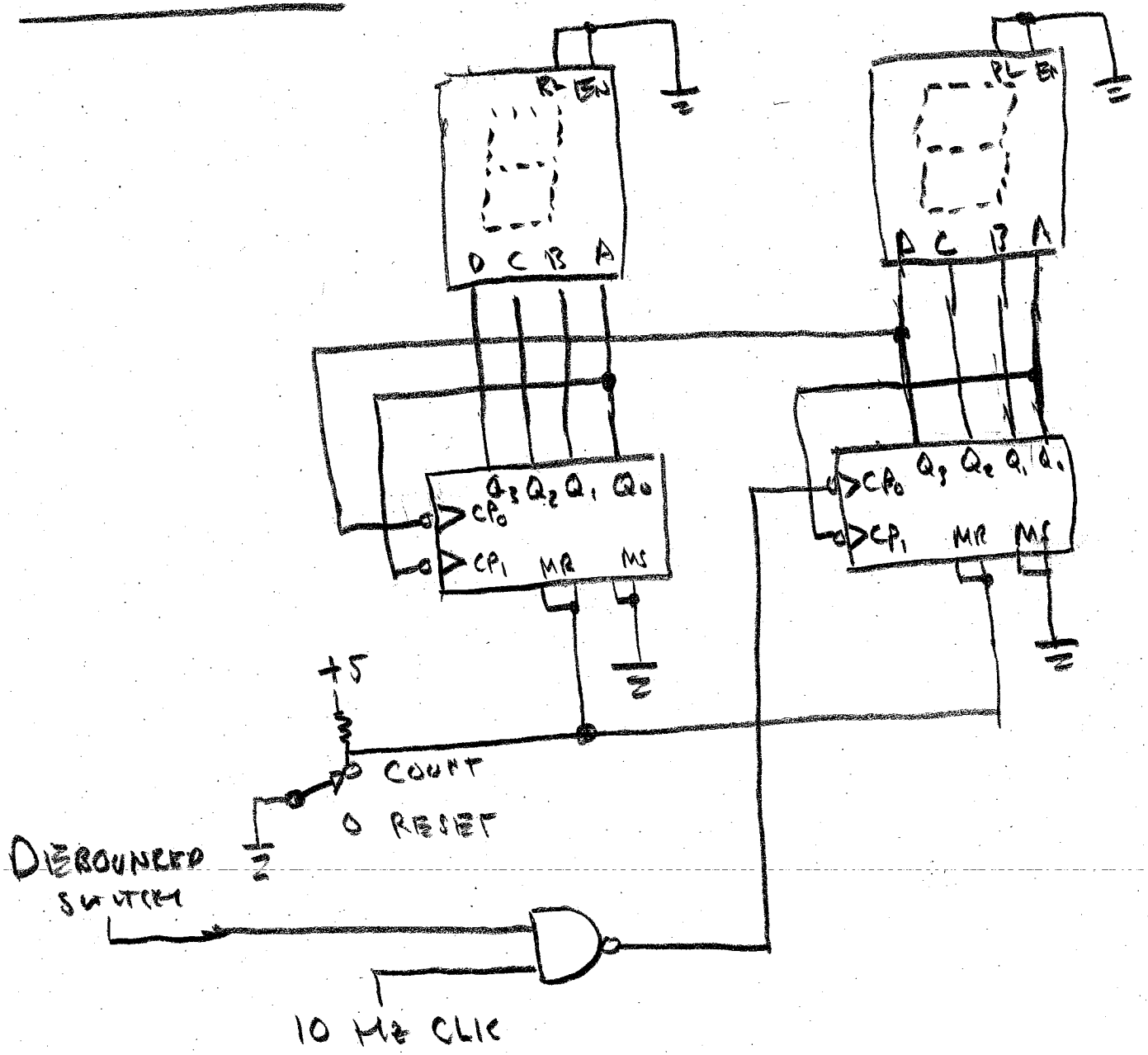


Figure 7

STOPWATCH


PL
EN
D C B A
Q_3 Q_2 Q_1 Q_0
CP_0
CP_1
MR
MS
+5
COUNT
RESET
DEBOUNCED SWITCH
10 MHz CLK

HEX DISPLAYS — USE TRANSPARENT LATCH & DECODE 4 bits to HEX.

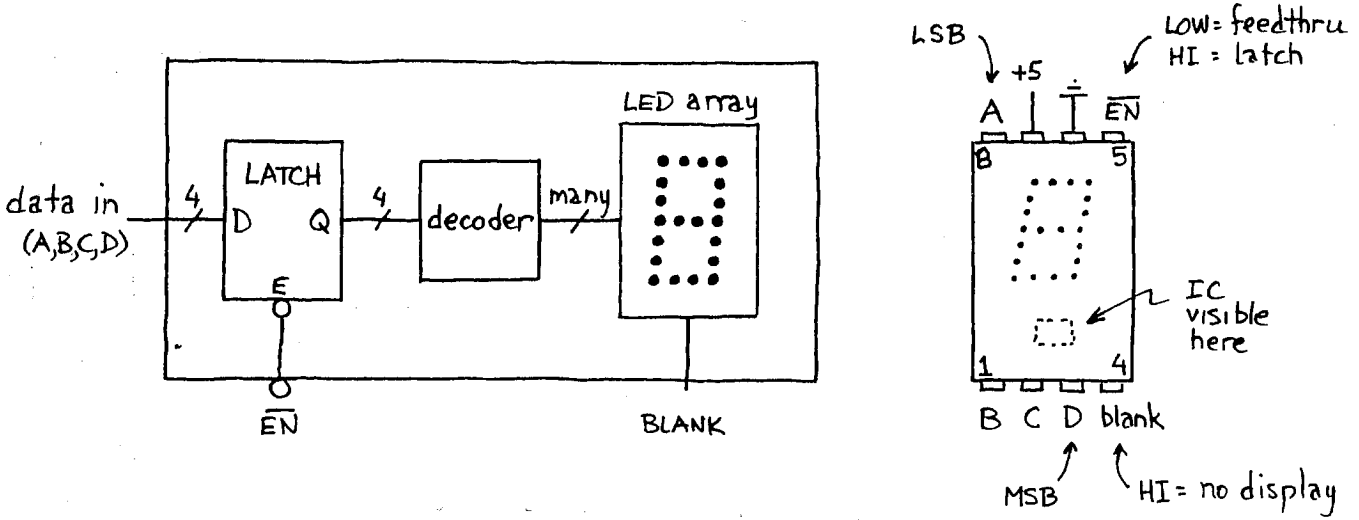


Figure L15.4: Hexadecimal display: pinout & functions