Physics 335
Lab 3 – MSI Counters, Binary Number Systems, and Displays

In this lab we will build a decade counter, a hexadecimal counter, a programmable divide-by-N counter, and a stopwatch.

Again, as before:

- Use the +5V Fixed Supplies with the negative terminal to ground and bypassed with a 0.1μF Capacitor on the breadboard.
- Before beginning, wire up the "debounced switch", which you will find in the drawers. The chip and all resistors are wired. Just connect power to pin 14, ground to pin 7, and add the toggle switches. A diagram is shown on the last page of this write-up.

3-1 MSI Counters & Displays

(A) The LS90

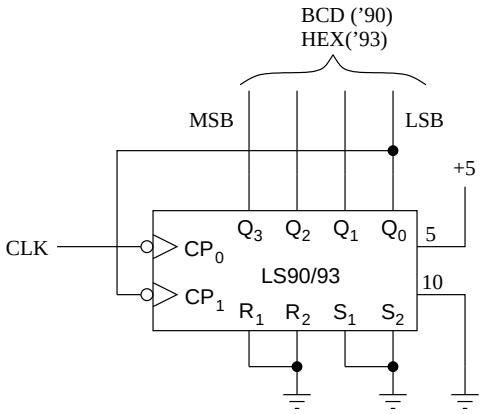
The 74LS90 and 74LS93 are a pair of pin-for-pin compatible counters, except the LS90 is a decade counter, and the LS93 is a hexadecimal (true binary) counter. These chips have unusual power connections: V_{cc} = Pin 5; GND = Pin 10.

Look up the data sheet for the LS90/93 chips (it is on the class website). From the datasheet, determine the pinouts for all of the signal connections (inputs and outputs). When you draw your diagram, indicated the pin numbers on it. It is a good idea to do this before wiring it up!

Wire up the LS90 chip as shown. Avoid running wires over the top of the chip. Later You will be replacing with the pin compatible HEX counter 74LS93. The chips are actually 2 separate counters, a divide-by-two section "0" and a divide-by-five section "2" for the '90 and a divide-by-8 section for the '93. Each section has a separate, independent clock input: CP_0 and CP_1.

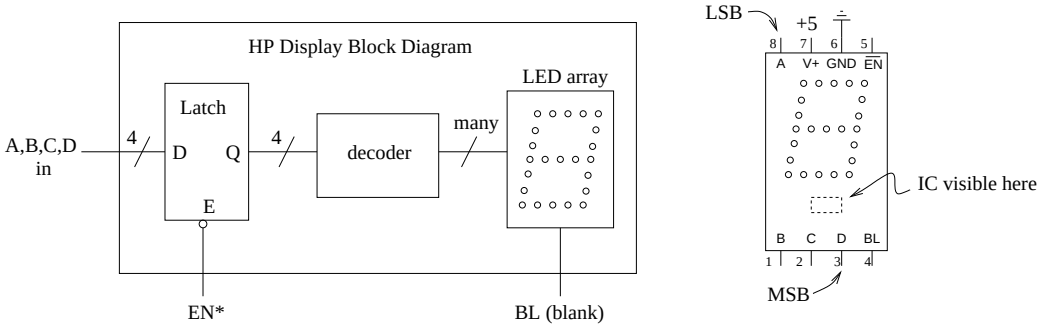
Use the 4-LED array to look at the BCD output while clocking the input with the debounced switch. (See the last page for a diagram) Take the resets R_1 and R_2 off ground and figure out what it does, then do the same with sets S_1 and S_2.

Is this a synchronous or a ripple counter and how do you determine this?



(B) HP Display Chip

Use one section of the HP Display Chip assembly (in the "Display" drawer) to look at the counter outputs. ***These display chips are very expensive, so be careful about wiring the power up!***



The display chip is more than just a seven segment LED, It has a *decoder* that translates the binary number input to A, B, C and D into the proper pattern, and it includes a *transparent latch* that allows the number to be loaded on the assertion of EN* and saved when EN* is disasserted (note "assert" means "set to LOW"). There is also a *blank* pin that when asserted will cause the LEDs to turn off. You can see the IC in the face of the chip that tells you which side is down.

Wire up the display to the counter outputs and count through the states manually toggling the debounced switch. Note that it will count only on one edge of the clock, thus you must cycle the switch fully (back and forth) for each step.

(C) The LS93

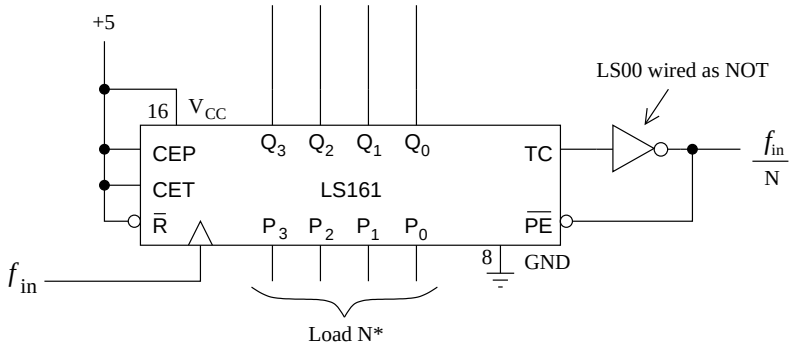
Now turn off the power and pull out the the 74LS90 and replace it with a '93 (HEX counter) It is pin compatible but there is no S_1, S_2 connections (pins 6 and 7). Step through the count and record your observations.

Use the TTL output of the function generator to clock faster. Look at the outputs Q_0 to Q_3 of the 93 in turn with the scope while you apply 1 kHz to the clock line and verify that each is half of the previous one.

Then pull out the '93, put back the '90 and do the same and justify what you see. Can you think of a way to use a '90 to give you a symmetrical square wave at one-tenth the frequency? Try out your idea (if you get one!)

3-2 **Programmable Divide-by-N Counter**

The LS161 and LS163 are 4 bit synchronous binary (divide-by-16) and the LS160 and LS162 are decade (divide by 10) counters. They either have synchronous ('162, '163) or jam (= master = asynchronous) resets ('160, '161). They can be direct parallel-loaded synchronously (on the rising edge of the clock) from the data inputs P_0 through P_3 enabled by the "LOAD": PE*. The chips also put out a carry out (i.e., "terminal count", TC) which goes high when the '161 & '163 reach 15 or the '160 & '162 reach 9. With this feature, we can construct a divide-by-N programmable counter. We put $N*$ (the 2's complement of N) into the data inputs and enable load with the CT*.

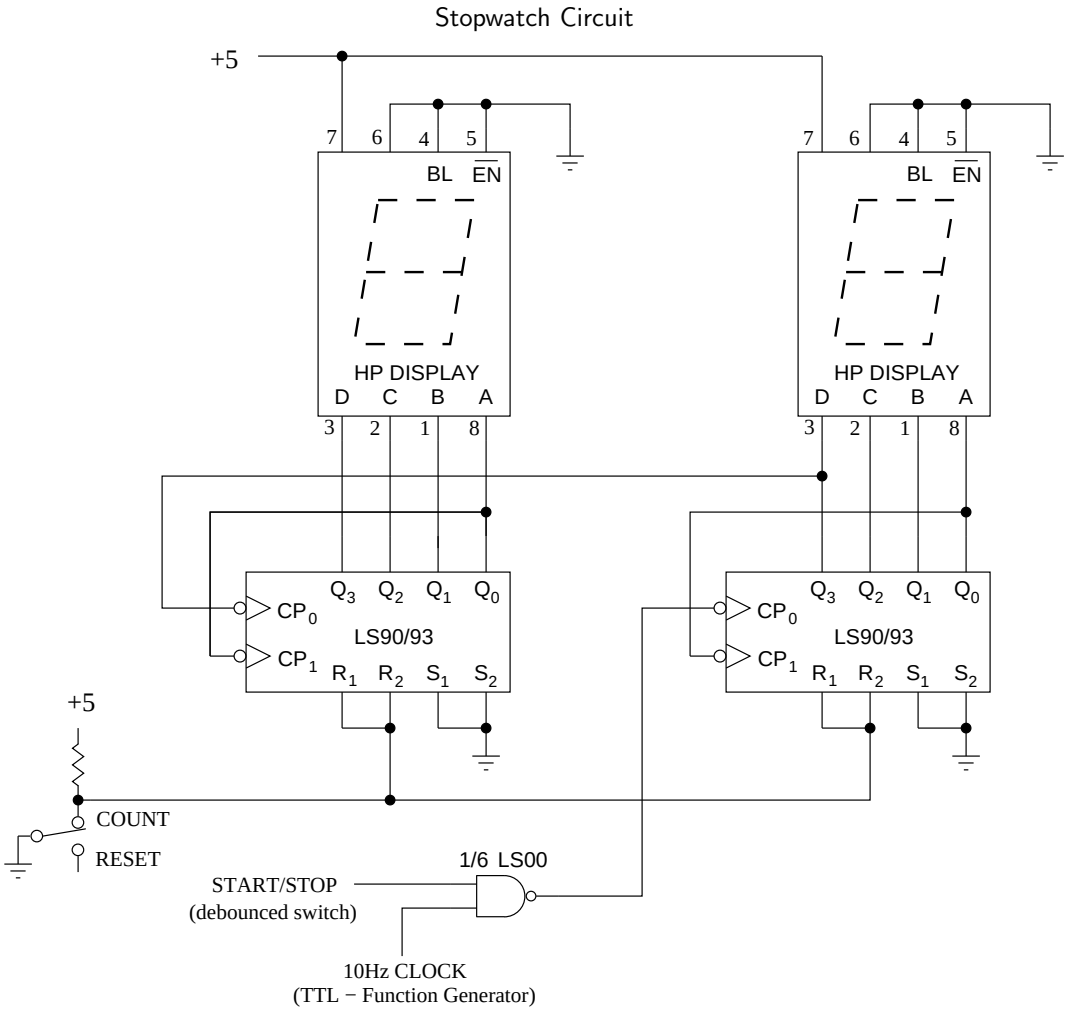


As before, look up the datasheet for the LS161 and determine its pinout and use it to wire up the circuit above. Use a debounced switch or the SYNC OUT of the function generator for f_{in} Use the HP display or the 4-LED array (your choice). For the inverter, use a 74LS00 wired appropriately.

- What is N* (2's complement of N) for a divide by 4 counter? Remember 2's complement is 1's complement plus 1.
- What logic levels should be applied to P_0–P_3 for a divide by 6 counter?
- What frequency should a divide-by-4 and a divide-by-6 counter output if we apply f =10kHz to the clock input. Look at the output on TC (pin 15). Why isn't the waveform symmetric?

3-3 A Stopwatch

The last project today is a stopwatch made from cascaded BCD counters (LS90s) running from a 10Hz clock signal supplied by the function generator. Gate the clock into the counter with a 74LS00 as shown. Use a second switch to reset the counter.



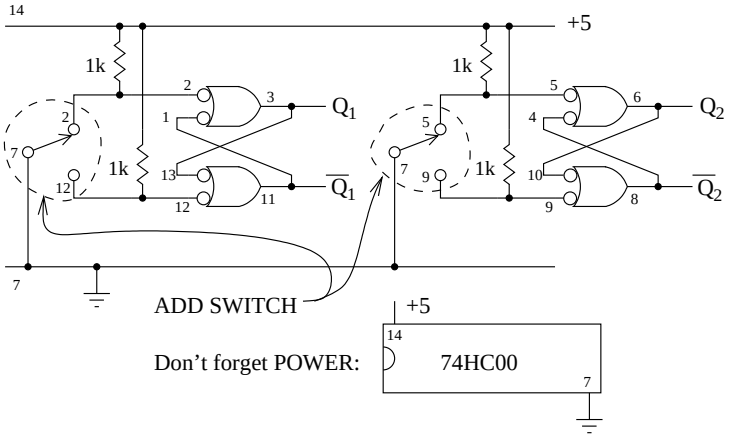
This takes about an hour to do, so don't start unless you have time.

Wire neatly to avoid troubleshooting headaches.

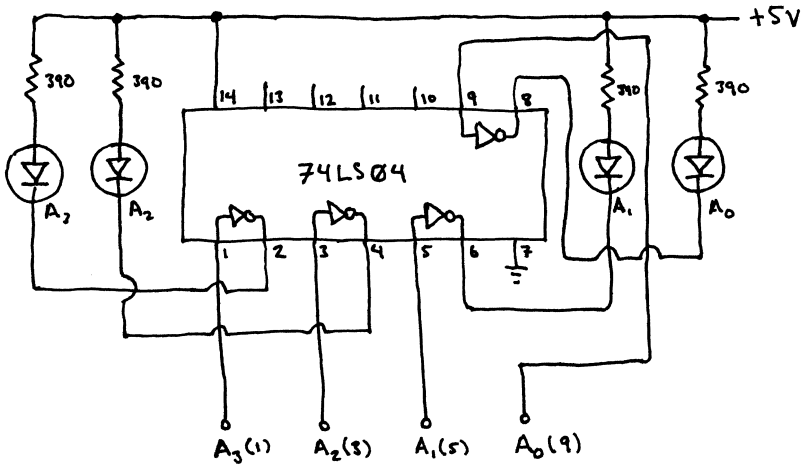
Questions:

- Why is it necessary to debounce the gates switch but not the reset switch?
- Which counter is the MSB? LSB?
- Notice Q_3 goes high at binary 1000 (8) of the LSB, but we don't want to increment the MSB until after 1001 (9). Why doesn't this pose a problem for us?

PARTIALLY PRE-WIRED DEBOUNCED SWITCHES



PRE-WIRED FOUR LED ARRAY



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Parts adapted from *The Student Manual for the Art of Electronics*
by Thomas C, Hayes and Paul Horowitz (Cambridge University, 1989)
`Lab3_Counters_14.tex -- Updated 18 April 2014`