Physics 335
Lab 2 – Flip Flops and Intro to Sequential Logic

Use only the fixed +5V outputs from the lab power supplies. As before, bring the voltages out to the strips on the breadboard and bypass the supply voltages with 0.1 μF capacitors. (Always do this as a matter of good practice—it makes the power source look like the low-impedance voltage source it should at all frequencies.)

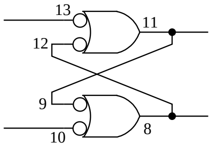
Be sure to connect all unused CMOS inputs to +5V or ground!

2-1 Primitive Flip-Flop: NAND Latch

Build the latch circuit shown below using the 74LS00 (TTL) so you don't need to worry about the unused inputs. Look at the pinout diagram on the laminated sheets in the lab and make a circuit diagram of the latch that shows which pins you use before wiring it up (it will help you avoid wiring mistakes.

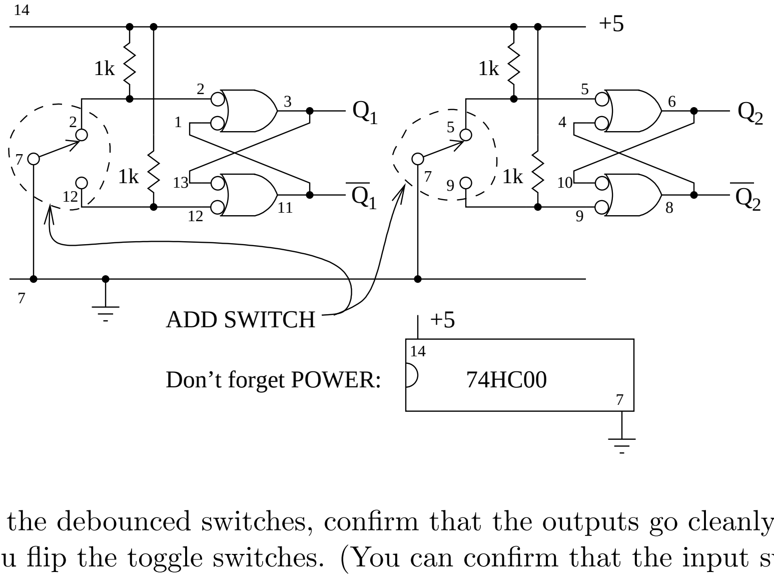
Don't forget to supply power to pins 14 and 7! (A surprisingly common mistake.)

To set the input HI or LO just plug wires into +5 or ground at the inputs. Make a complete truth table using the logic probe and determine which input combination determines the "memory" or bistable state.



For the rest of the lab we will need 2 "debounced" switches. There are partially wired switches available in the parts bins: a 74HC00 chip plugged into a socket and wired according to the diagram below. It is in a separate drawer of special parts marked "Debounced Switch" (and other things). You ONLY need to hook up the power and plug the toggle switches into the appropriate points; the rest of the connections are already made. The outputs of these will be used to reliably clock the flip-flop circuits.

PARTIALLY PRE-WIRED DEBOUNCED SWITCHES



After wiring up the debounced switches, confirm that the outputs go cleanly between HIGH and LOW as you flip the toggle switches. (You can confirm that the input switches actually bounce if you trigger the 'scope on the output of the debouncing circuit while watching one of the inputs to the latch circuit. You will need a pretty high sweep rate on the scope to see the "trash" on the input.) Hint: set the trigger to NORMAL, and trigger on the output of the latch.

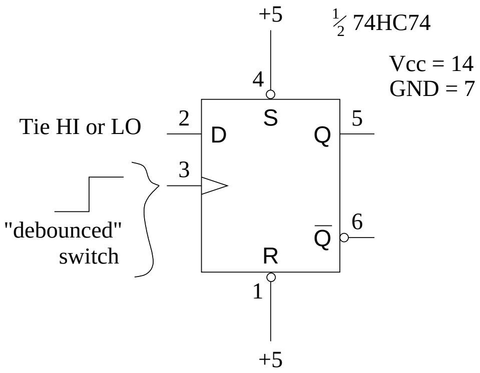
2-2 D Type Flip-Flop

The D type flip flop simply saves the state of the input (D = "data") when the clock input changes state. It seems sort of dull at first, but it becomes the most important type of flip-flop of all when used in real circuits.

Use a 74HC74 chip (CMOS), and remember to wire the unused inputs to ground or +5 (it doesn't matter which). The inputs are the $\overline{S}$, $\overline{R}$ D *and* clock (▷) lines (pins 1, 4, 10, 11, 12, 13; see the pinout sheet in the lab).

a) Saving a level; using Set & Reset

Set up one of the flops for testing (there are two per package) with one debounced switch wired into the D input and the other hooked to the clock input.



Try the following:

- Confirm that the output ignores whatever is on the D line until the flop is clocked.
- Try asserting Reset* ($\overline{R}$). ("Assert" means "make LOW" here, remember?) What happens if you clock the flop when $\overline{R}$ is asserted?
- Do the same with Set* ($\overline{S}$).
- Try asserting both Set* and Reset* at the same time (something you would never do on purpose otherwise) What happens? Look at both outputs. What would happen if both were disasserted at once?

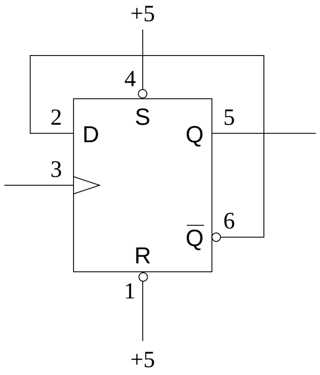
Note: we use both an asterisk (*) and a prime (′) to denote inversion: $\overline{S} \equiv S* \equiv S'$.

With the above, and a bit more, confirm the following truth table:

$\overline{S}$	$\overline{R}$	clock	D	Q
H	H	↑	H	H
H	H	↑	L	L
H	H	↓	X	unch.
L	H	X	X	H
H	L	X	X	L
L	L	X	X	?

b) Toggle connection: Feedback

Wire up the circuit below (you only need to add one wire) and clock the flop manually with the debounced switch. Count how many times you need to flip the switch for Q to change.



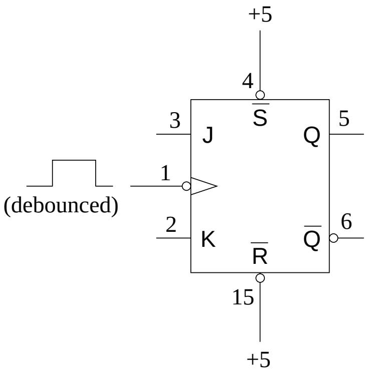
Remove the manual clock connection and clock the flop with the TTL output of the function generator (SYNC). Watch both the clock and Q lines on the 'scope and draw the two waveforms you see. Why is this circuit called a "divide-by-two"?

To see the *propagation delay*, you will need to increase the scope's sweep rate and generator's frequency. Make sure to trigger on the clock input only. Compare what you get for propagation delay to the specifications for the part. A spec sheet is given online at the course website or you can find one at www.datasheetcatalog.com.

NOTE: If you see funny wiggles right at the edges of the transitions, you should be able to reduce these by (1) adding a capacitor across the power input lines (7 and 14) near the chip (0.1 μF should do) and (2) connecting the ground of the scope probe close to the ground near the chip. (Use a bonafide *'scope probe*, not BNC adapters plus bare wires coming from binding posts.)

2-3 J-K Type Flip-Flop

Wire up the 74HC112 J-K type and discover the truth table (see the next page). Again: there are two per package (here 16 pins), wire unused inputs to +5V or ground, and don't forget the power connections to pins 8 and 16.



Be sure to wire the $\overline{S}$ and $\overline{R}$ inputs of both flops in the package to high. See the pinout diagram on the laminated sheets in the lab ("CLR" is the same as $\overline{R}$).

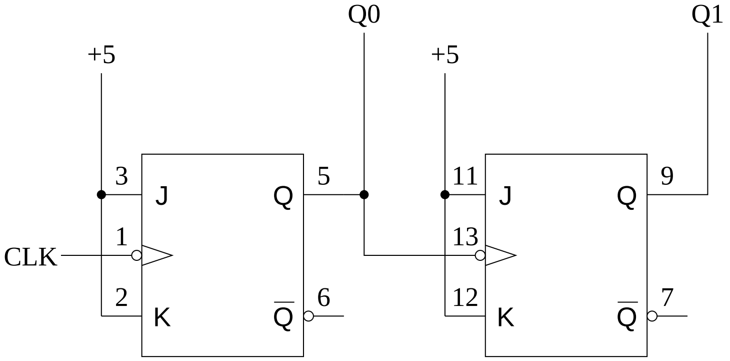
J	K	Q_n	Q_{n+1}

Note that "Q_n" means the state of Q immediately before the clock edge and "Q_{n+1}" means the state of the output Q following clock edge n.

2-4 Two-Bit Counters

(A) Ripple Counter

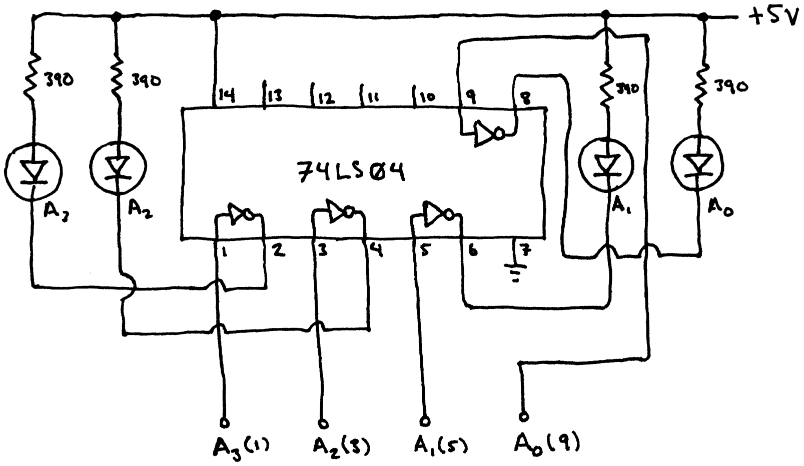
Wire the two J-K flops as shown below.



Check that $\overline{S}$ and $\overline{R}$ are disasserted for both flops (they should be, already).

Locate the pre-wired LED array in your parts drawer and plug it in to your breadboard. You need to attach the power only (as usual, to pins 14 and 7). Then connect two inputs of the LED array to the Q_0 and Q_1 outputs (e.g, to pins 9 and 5, A_0 and A_1).

PRE-WIRED FOUR LED ARRAY



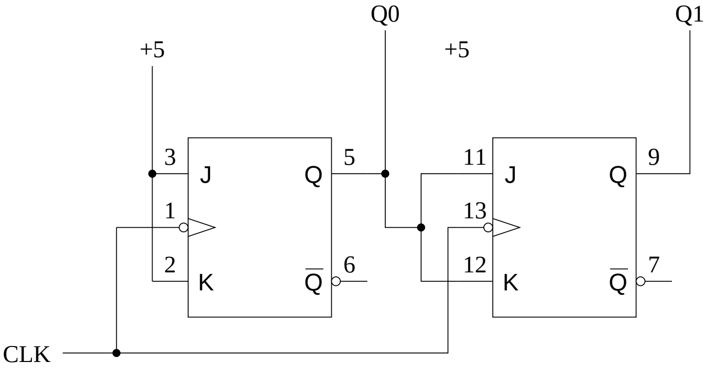
Connect the clock input to the TTL output on the function generator, and look first at the behavior of the LED lighting when the frequency is set at about 1 Hz (or a bit higher). Does it “divide by four?” (If it doesn’t, there is a problem.)

Clock the counter at high frequency and look at the outputs on the ’scope. Draw comparative waveforms of the clock input, Q_0 and Q_1. (Hint: trigger on Q_1.)

Finally, crank the frequency up until you can see the effect of propagation delay on the two waveforms. Again, you may need to add a bypass capacitor d b careful about the ground lead to your scope probe.

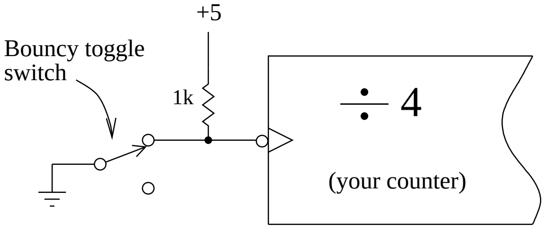
(B) Synchronous counter

Make the small change to turn the counter into a synchronous type, and compare the high frequency waveform with what you saw with the ripple counter. In particular, notice the absence of delay between the 1’s and 2’s column waveforms.



2-5 Switch Bounce

Connect a toggle switch directly to the clock line, as shown below. Note the use of a pullup resistor to raised the voltage up to +5V when the switch is open.



Watch the LEDs and notice how the number advances when you flip the switch. Do you always advance by 1 when the switch is closed (negative edge)? You may have to flip the toggle vigorously to see the odd effect. Our little SPDT switches are not as “bouncy” as some types.

Compare the action you see here with what you got from the debounced switch.

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Parts adapted from *The Student Manual for the Art of Electronics*
by Thomas C, Hayes and Paul Horowitz (Cambridge University, 1989)
`Flip-flops_Lab2_14.tex -- Updated 11 April 2014`