Physics 335, Spring Quarter 2013
Electric Circuits II
Reading Assignments

Week 1 Reading 1-5 April
Textbook section 8.01 (overview of digital vs. analog), section 8.02 (for now, browse only the paragraphs under "high & low", pp472-3), section 8.03 (number codes, especially "hex" numbers for the homework), section 8.04 (gates & truth tables), section 8.05 (discrete circuits for gates, especially note fig 8.8 appears in the lab next week), section 8.10 (TTL & CMOS input and output characteristics), section 8.11 ("3-state" & open-collector outputs).

Week 2 Reading 8 – 12 April
There's a confusing situation regarding the different voltages for input "true" and "false" for TTL and CMOS logic; this is summarized in textbook p. 475 "logic levels"; notice the logic-analyzer you use in lab can switch between TTL and CMOS input logic levels. Look at textbook section 8.12 (overview of logic identities). Glance at section 8.14 (the discussion of the Transmission Gate, a device you've seen in Phys 334…this is very useful for digital control of analog signals). Section 8.16 (sequential logic…the whole section is going to be covered…except the subtlety of master-slave vs edge-triggered). Section 8.18 (combining gates and flip-flops. In Glancing at flip-flops, note how cumbersome it is to divide by a non-power-of-2).

Week 3 Reading 15 – 19 April
Last Thursday we started the topic of sequential logic; Tuesday is more detail on this. In particular, we'll cover the "D-latch" and the "J/K flip flop" pages 508-510 in the text (including the divide-by-2 page 510) in the text. Thursday we'll talk about "ripple" versus "synchronous" counters. We'll then make a clumsy "divide-by-n" counter, where "n" isn't necessarily a power of 2; note how cumbersome it is to divide by a non-power-of-2).

Week 4 Reading 22-26 April
Textbook section 8.20 and 8-22 (“one-shots”; monostables): Read especially the introduction (p. 517) and 8.20. You should look this over as you could use it for the homework due Tuesday. Glance at the discussion of retriggerability; there’s also a question about retriggerability on the homework. In lecture we’ll discuss the 74121 (fig. 8.64). Personally, I rarely use one-shots; I tend to instead make digital delays (see “general considerations” p. 521). We’ll then start on interfacing digital with analog systems, starting with the Digital to Analog Converter (DAC).

Week 5 Reading 29 April-03 May
We’ll continue from last Thursday’s lecture on interfacing digital with analog systems with the Digital to Analog Converter (DAC); textbook section 9.16: we’ll wrap up the “R-2R” type as that’s most common. We’ll then discuss Analog to Digital Converters (ADCs), with focus on the “flash” and “successive approximation” types. ADC’s of the “flash” and “half-flash” types are on the homework.

Week 6 Reading 06–10 May
We’re starting the second half of the course, where the focus shifts to micro-controllers. Start by reading the textbook pp 673-678; this is an overview of computer architecture. Then read textbook section 10.02; this is an introduction to assembly language programming. You can continue reading the textbook, but it moves into programming the Motorola 68k microprocessor, which we won’t be using. Now shift reading to the PIC 16F84A datasheet on the course web site (see the “datasheets” at the upper left): Try to get an overview of this microcontroller. Page 1 is an overview of the chip’s architecture. Section 1.0 gives a more detailed chip architecture overview. Section 2 describes the data and program memories. The data memory also includes “special function registers”; in lecture and lab, we’ll be using the PORTB and TRISB registers, among others, to light LEDs and read the state of switches. You don’t need to absorb this datasheet all at once; for now just get familiar with it.

Week 7 Reading 13-17 May
There's an exam on Thursday. Reading: Continue looking at the PIC 16F84A datasheet. Section 7 of the datasheet describes the PIC operation codes ("op-codes" or instructions). Figure 7.1 describes how instructions are "assembled" into binary instructions for downloading into program memory. Table 7.2 is the relatively short list of PIC instructions, look it over. Except for the strange instructions like SLEEP and RETFIE, you should be able to make sense of what the instructions do.

Week 3 Reading 20-24 May
Reading: We'll continue looking at the PIC 16F84A datasheet. In class ,we'll go over a simple example of a look-up table using the CALL-RETLW pairing. We'll then "dis-assemble" a move instruction for the PIC processor and for a fancier microprocessor (this uses information from the datasheet Figure 7.1). We'll then talk about interrupts or "exception handling". Section 10.09 through 10.11 in the textbook covers interrupts, though it can be tough reading. The PIC has a simpler interrupt architecture, and we'll look at an example.

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