Physics 335, Spring Quarter 2011, Examination

Name SOLUTIONS V1.2

1	/35
2	/35
3	/30
TOTAL	/100

Please check that you have a total of 7 exam pages, including this page.

This exam is closed-book. There's a summary of PIC instructions on the following page.

TABLE 7-2: PIC16CXXX INSTRUCTION SET

Mnemonic, Operands		Description	Cycles	14-Bit Opcode MSb			LSb	Status Affected	Notes
BYTE-ORIENTED FILE REGISTER OPERATIONS									
ADDWF	f, d	Add W and f	1	00	0111	dfff	ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00	0101	dfff	ffff	Z	1,2
CLRF	f	Clear f	1	00	0001	lfff	ffff	Z	2
CLRW	-	Clear W	1	00	0001	0xxx	xxxx	Z	
COMF	f, d	Complement f	1	00	1001	dfff	ffff	Z	1,2
DECF	f, d	Decrement f	1	00	0011	dfff	ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1 (2)	00	1011	dfff	ffff		1,2,3
INCF	f, d	Increment f	1	00	1010	dfff	ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1 (2)	00	1111	dfff	ffff		1,2,3
IORWF	f, d	Inclusive OR W with f	1	00	0100	dfff	ffff	Z	1,2
MOVF	f, d	Move f	1	00	1000	dfff	ffff	Z	1,2
MOVWF	f	Move W to f	1	00	0000	lfff	ffff		
NOP	-	No Operation	1	00	0000	0xx0	0000		
RLF	f, d	Rotate Left f through Carry	1	00	1101	dfff	ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00	1100	dfff	ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00	0010	dfff	ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00	1110	dfff	ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00	0110	dfff	ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS									
BCF	f, b	Bit Clear f	1	01	00bb	bfff	ffff		1,2
BSF	f, b	Bit Set f	1	01	01bb	bfff	ffff		1,2
BTFSC	f, b	Bit Test f, Skip if Clear	1 (2)	01	10bb	bfff	ffff		3
BTFSS	f, b	Bit Test f, Skip if Set	1 (2)	01	11bb	bfff	ffff		3
LITERAL AND CONTROL OPERATIONS									
ADDLW	k	Add literal and W	1	11	111x	kkkk	kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11	1001	kkkk	kkkk	Z	
CALL	k	Call subroutine	2	10	0kkk	kkkk	kkkk		
CLRWDT	-	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}$,$\overline{PD}$	
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
IORLW	k	Inclusive OR literal with W	1	11	1000	kkkk	kkkk	Z	
MOVLW	k	Move literal to W	1	11	00xx	kkkk	kkkk		
RETFIE	-	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	01xx	kkkk	kkkk		
RETURN	-	Return from Subroutine	2	00	0000	0000	1000		
SLEEP	-	Go into standby mode	1	00	0000	0110	0011	$\overline{TO}$,$\overline{PD}$	
SUBLW	k	Subtract W from literal	1	11	110x	kkkk	kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11	1010	kkkk	kkkk	Z	

1. (35 points) PIC 16F84A programming.
Find the value of w-register after execution of the following snippets of code. You can assume the 16f84a.inc definitions are loaded. Put your answer in hexadecimal form in the box.

```
movlw B'00001111' ;move literal to w
```

w (hex) = H'0F' [= B'0000 1111']

```
movlw H'06' ;move literal to w
andlw H'04' ;Boolean literal and to w
```

w (hex) = H'04' [= B'0000 0100']

```
movlw H'06' ;move literal to w
movwf H'0E'; move w to file register
bsf H'0E', H'03' ;bit set
movf H'0E', w ;move file register
```

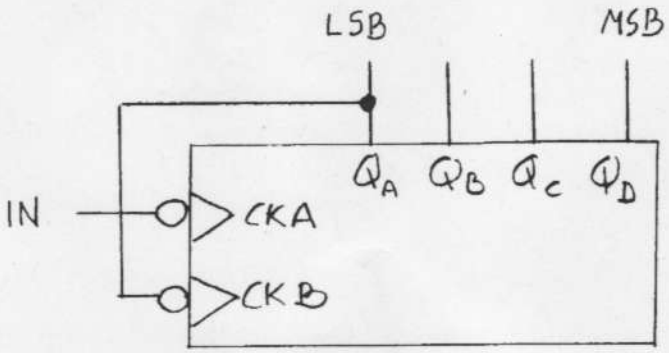
w (hex) = H'0E' [= B'0000 1110']

NOTICE IT'S A TRICK QUESTION- THIS INSTRUCTION DOESN'T MODIFY W,

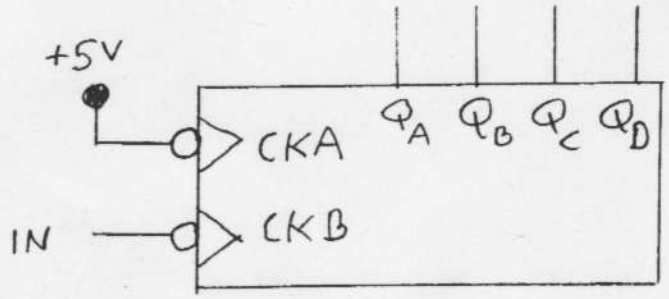
```
movlw H'06' ;move literal to w
movwf H'0E'; move w to file register
bsf H'0E', D'00' ;bit set
movf H'0E', f ;move file register
```

w (hex) = H'06' [= B'0000 0110']

2. (35 points) Counters. Recall in lab we used a 74LS90 configured as shown just below as a decade counter. Also recall that the connection between output Q_A and input CKB was made because this counter has two independent counters, a divide-by-two counter (clocked at CKA with output Q_A) and a divide-by-five counter (clocked at CKB with outputs Q_B, Q_C and Q_D).



Now, from this point on, consider the 74LS90 wired as shown below. Assume un-shown inputs don't disable counting.



A. In 10 words or less, what's the "wedge" at CKA and CKB indicate?

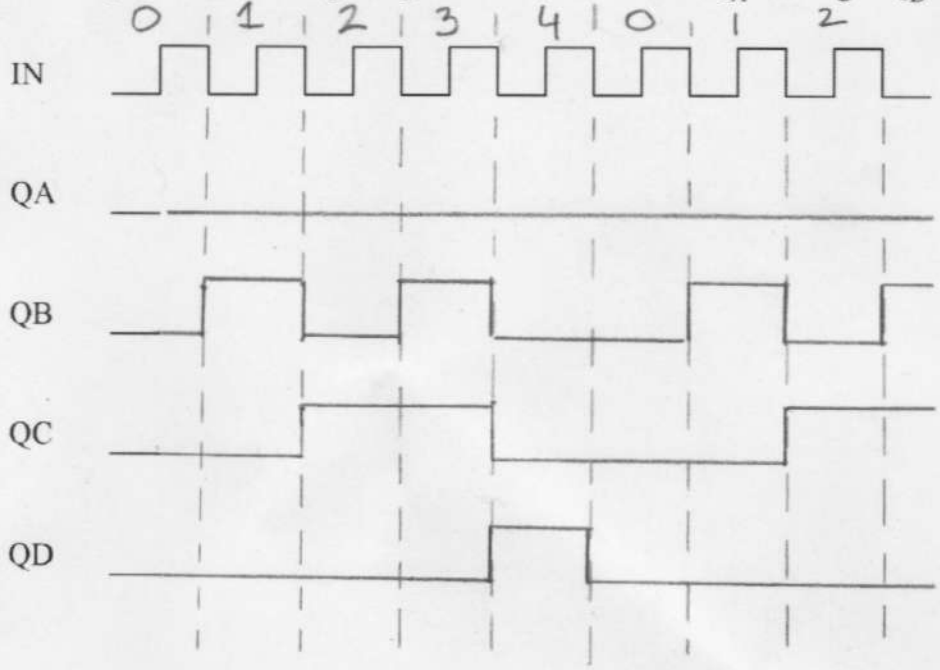
The wedge indicates ... EDGE-TRIGGERED INPUT.

B. In 10 words or less, what's the "open ball" at CKA and CKB indicate?

The open ball indicates ... TRIGGER ON FALLING EDGE.

(problem 2, continued)

C. Complete the timing diagram below. Notice Q_A through Q_D start "low".

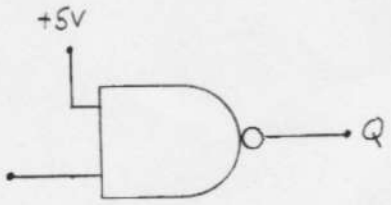


D. In 10 words or less, describe a simple wiring modifications to this circuit, that, without adding any additional gates or parts, produces a symmetric duty-factor decade counter.

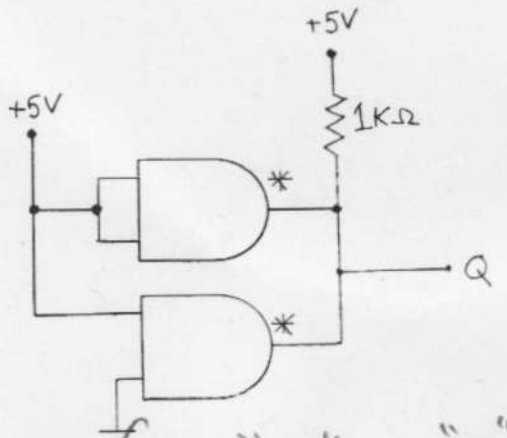
You simply ... CONNECT Q_D TO CLKA AND USE QA AS THE OUTPUT;
OR YOU CAN CONNECT Q_C TO CLKA AND USE QA AS OUTPUT.

3. (30 points) Digital circuits: short answers.

A. Single gate: what's the value of Q? $Q = \overline{A}$



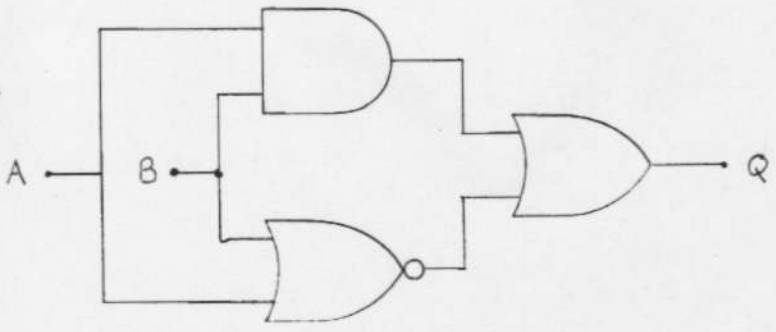
B. Two open-collector logic gates are wired as shown.



What's the value of Q? Q = LOW {OR "F" OR "0" OR 0V.}

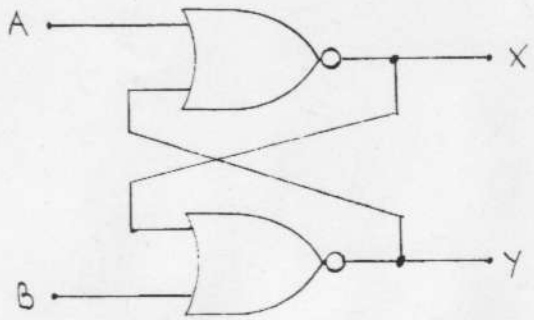
C. Fill in the truth table (positive logic)

A	B	Q
0	0	1 {OR "T", etc.}
0	1	0
1	0	0
1	1	1



D. Fill in the truth table, assuming A, B = 1, 1 is followed by 1, 0 then 0, 1 etc. (positive logic)

A	B	X	Y
1	1	0	0
1	0	0	1
0	1	1	0
1	0	0	1



E. D-latch: Fill in the timing diagram for Q with CLK and D as shown. Notice that Q starts low. Assume un-shown inputs don't inhibit clocking the chip.