SOLUTIONS V1.0

Physics 335, Circuits II: Digital Electronics
Spring Quarter 2013
Mid-Term Examination

Name _____

1	/20	
2	/25	
3	/35	
4	/20	
TOTAL	/100	

Please check that you have a total of 11 printed pages, including this page.

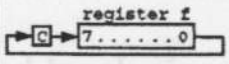
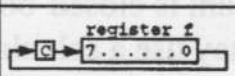
Exam notes: This exam is closed-book. No laptops, tablet computers or smartphones. You may use a calculator. On the following few pages, there's a summary of PIC instructions, a memory map of the PIC hardware registers, and a description of the PIC status register. You can use scratch paper, but the scratch paper won't be graded.

14-Bit Core Instruction Set

14-Bit Core Literal and Control Operations

Hex	Mnemonic		Description	Function
3Ekk	ADDLW	k	Add literal to W	k + W → W
39kk	ANDLW	k	AND literal and W	k .AND. W → W
2kkk	CALL	k	Call subroutine	PC + 1 → TOS, k → PC
0064	CLRWDT	T	Clear watchdog timer	0 → WDT (and Prescaler)
2kkk	GOTO	k	Goto address (k is nine bits)	k → PC(9 bits)
38kk	IORLW	k	Incl. OR literal and W	k .OR. W → W
30kk	MOVLW	k	Move Literal to W	k → W
0062	OPTION		Load OPTION register	W → OPTION Register
0009	RETFIE		Return from Interrupt	TOS → PC, 1 → GIE
34kk	RETLW	k	Return with literal in W	k → W, TOS → PC
0008	RETURN		Return from subroutine	TOS → PC
0063	SLEEP		Go into Standby Mode	0 → WDT, stop oscillator
3Ckk	SUBLW	k	Subtract W from literal	k - W → W
006f	TRIS	f	Tristate port f	W → I/O control reg f
3Akk	XORLW	k	Exclusive OR literal and W	k .XOR. W → W

14-Bit Core Byte Oriented File Register Operations

Hex	Mnemonic		Description	Function
07ff	ADDWF	f,d	Add W and f	W + f → d
05ff	ANDWF	f,d	AND W and f	W .AND. f → d
018f	CLRF	f	Clear f	0 → f
0100	CLRW		Clear W	0 → W
09ff	COMF	f,d	Complement f	.NOT. f → d
03ff	DECF	f,d	Decrement f	f - 1 → d
0Bff	DECFSZ	f,d	Decrement f, skip if zero	f - 1 → d, skip if 0
0Aff	INCF	f,d	Increment f	f + 1 → d
0Fff	INCFSZ	f,d	Increment f, skip if zero	f + 1 → d, skip if 0
04ff	IORWF	f,d	Inclusive OR W and f	W .OR. f → d
08ff	MOVF	f,d	Move f	f → d
008f	MOVWF	f	Move W to f	W → f
0000	NOP		No operation	
0Dff	RLF	f,d	Rotate left f	
0Cff	RRF	f,d	Rotate right f	
02ff	SUBWF	f,d	Subtract W from f	f - W → d
0Eff	SWAPF	f,d	Swap halves f	f(0:3) ↔ f(4:7) → d
06ff	XORWF	f,d	Exclusive OR W and f	W .XOR. f → d
1bff	BCF	f,b	Bit clear f	0 → f(b)
1bff	BSF	f,b	Bit set f	1 → f(b)
1bff	BTFSC	f,b	Bit test, skip if clear	skip if f(b) = 0
1bff	BTFSS	f,b	Bit test, skip if set	skip if f(b) = 1

2.2 Data Memory Organization

The data memory is partitioned into two areas. The first is the Special Function Registers (SFR) area, while the second is the General Purpose Registers (GPR) area. The SFRs control the operation of the device.

Portions of data memory are banked. This is for both the SFR area and the GPR area. The GPR area is banked to allow greater than 116 bytes of general purpose RAM. The banked areas of the SFR are for the registers that control the peripheral functions. Banking requires the use of control bits for bank selection. These control bits are located in the STATUS Register. Figure 2-2 shows the data memory map organization.

Instructions MOVWF and MOVF can move values from the W register to any location in the register file ("F"), and vice-versa.

The entire data memory can be accessed either directly using the absolute address of each register file or indirectly through the File Select Register (FSR) (Section 2.5). Indirect addressing uses the present value of the RP0 bit for access into the banked areas of data memory.

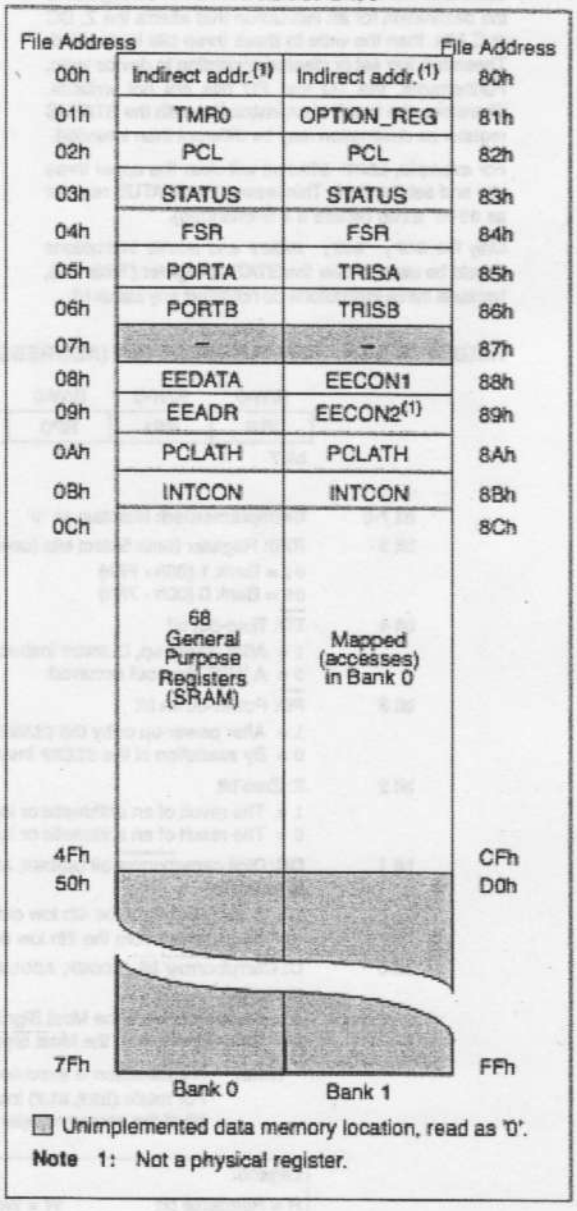
Data memory is partitioned into two banks which contain the general purpose registers and the special function registers. Bank 0 is selected by clearing the RP0 bit (STATUS<5>). Setting the RP0 bit selects Bank 1. Each Bank extends up to 7Fh (128 bytes). The first twelve locations of each Bank are reserved for the Special Function Registers. The remainder are General Purpose Registers, implemented as static RAM.

2.2.1 GENERAL PURPOSE REGISTER FILE

Each General Purpose Register (GPR) is 8-bits wide and is accessed either directly or indirectly through the FSR (Section 2.5).

The GPR addresses in Bank 1 are mapped to addresses in Bank 0. As an example, addressing location 0Ch or 8Ch will access the same GPR.

FIGURE 2-2: REGISTER FILE MAP - PIC16F84A



2.3.1 STATUS REGISTER

The STATUS register contains the arithmetic status of the ALU, the RESET status and the bank select bit for data memory.

As with any register, the STATUS register can be the destination for any instruction. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to device logic. Furthermore, the $\overline{TO}$ and $\overline{PD}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, `CLRF STATUS` will clear the upper three bits and set the Z bit. This leaves the STATUS register as `000u uluu` (where `u` = unchanged).

Only the `BCF`, `BSF`, `SWAPF` and `MOVWF` instructions should be used to alter the STATUS register (Table 7-2), because these instructions do not affect any status bit.

Note 1: The IRP and RP1 bits (STATUS<7:6>) are not used by the PIC16F84A and should be programmed as cleared. Use of these bits as general purpose R/W bits is NOT recommended, since this may affect upward compatibility with future products.

2: The C and DC bits operate as a $\overline{borrow}$ and digit $\overline{borrow}$ out bit, respectively, in subtraction. See the `SUBLW` and `SUBWF` instructions for examples.

3: When the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. The specified bit(s) will be updated according to device logic

REGISTER 2-1: STATUS REGISTER (ADDRESS 03h, 83h)

R/W-0	R/W-0	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
IRP	RP1	RP0	$\overline{TO}$	$\overline{PD}$	Z	DC	C
bit 7							bit 0

bit 7-6 **Unimplemented:** Maintain as '0'

bit 5 **RP0**: Register Bank Select bits (used for direct addressing)
01 = Bank 1 (80h - FFh)
00 = Bank 0 (00h - 7Fh)

bit 4 **$\overline{TO}$**: Time-out bit
1 = After power-up, `CLRWDT` instruction, or `SLEEP` instruction
0 = A WDT time-out occurred

bit 3 **$\overline{PD}$**: Power-down bit
1 = After power-up or by the `CLRWDT` instruction
0 = By execution of the `SLEEP` instruction

bit 2 **Z**: Zero bit
1 = The result of an arithmetic or logic operation is zero
0 = The result of an arithmetic or logic operation is not zero

bit 1 **DC**: Digit carry/$\overline{borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions) (for $\overline{borrow}$, the polarity is reversed)
1 = A carry-out from the 4th low order bit of the result occurred
0 = No carry-out from the 4th low order bit of the result

bit 0 **C**: Carry/$\overline{borrow}$ bit (`ADDWF`, `ADDLW`, `SUBLW`, `SUBWF` instructions) (for $\overline{borrow}$, the polarity is reversed)
1 = A carry-out from the Most Significant bit of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note: A subtraction is executed by adding the two's complement of the second operand. For rotate (`RRF`, `RLF`) instructions, this bit is loaded with either the high or low order bit of the source register.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

1. (20 points total) Simple PIC 16F84A programming (I).
Find the value of w-register after execution of the following snippets of code. Assume the 16f84a.inc definitions are loaded. Express your answer as a hexadecimal number in the box.

(5 points)

```
movlw H'06'  ;move literal to w
addlw H'1E'  ;literal addition to w
```

w (hex) = H'24'

(5 points)

```
movlw H'06' ;move literal to w
iorlw H'1E' ;literal inclusive or with w
```

w (hex) = H'1E'

(5 points)

```
movlw H'06' ;move literal to w
andlw H'1E' ;literal and with w
```

w (hex) = H'06'

(5 points)

```
movlw H'0E'     ;move literal to w
movwf H'0E'     ;move w
xorwf H'0E',w   ;exclusive or
```

w (hex) = H'00'

2. (25 points total) Simple PIC 16F84A programming. (II)

(5 points) In the box below, write a sequence of no more than three instructions that do the same thing as the instruction shown (but don't use `clrf`):

```
clrf H'0F'
```

```
MOVLW H'00'
MOVWF H'0F'
(THERE ARE ALTORNATIVE WAYS
OF DOING THIS)
```

(10 points) In the box below, write a sequence of no more than three instructions that do the same thing as the instruction shown (but don't use `rrf`):

```
rrf H'0F',f
```

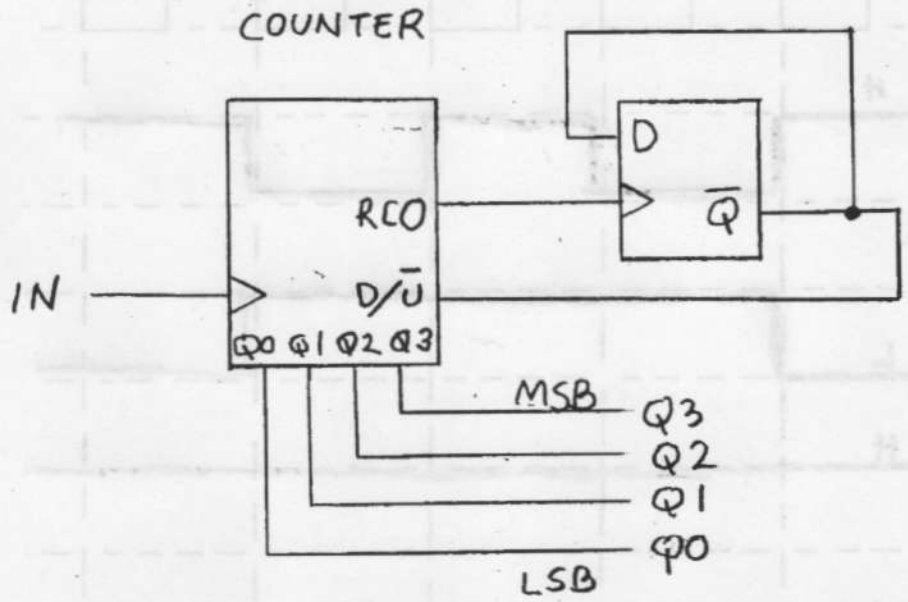
```
OPPS... I CAN'T FIGURE OUT HOW TO
DO THIS W/ JUST 3 INSTRUCTIONS,
EVERONE RECEIVES 10 POINTS FOR THIS
(APOLOGIES).
```

(10 points) Recall in class the `tris` instruction is depreciated; `tris` should be replaced by other instructions. Assume the instructions shown are executing while memory bank 0 is active. In the box below, write a sequence of no more than five instructions that do the same thing as the instructions shown (but don't use `tris`).

```
movlw H'00'
tris H'06'
```

```
BSF STATUS, RP0
CLRF TRISB
BCF STATUS, RP0
(THERE ARE ALTERNATIVE WAYS OF
DOING THIS)
```

3. (35 points total) Counters. The circuit below consists of a counter and a D-latch. The counter is similar to a 4-bit binary counter (with outputs Q0 through Q3) you used in lab, but there's an extra synchronous input "D/$\overline{U}$" which selects whether the counting is upwards or downwards. If counting upwards, the terminal count is decimal 15. If counting downwards, the terminal count is 0. RCO is the same "ripple carry-out" output you used in lab.



A. (2 points) What does the "wedge" at the counter input signify (10 words or less)?

The wedge signifies ... THE DEVICE STATE CHANGES ON A RISING CLOCK EDGE.

B. (5 points) What does it mean to say D/$\overline{U}$ is a "synchronous input" (10 words or less)?

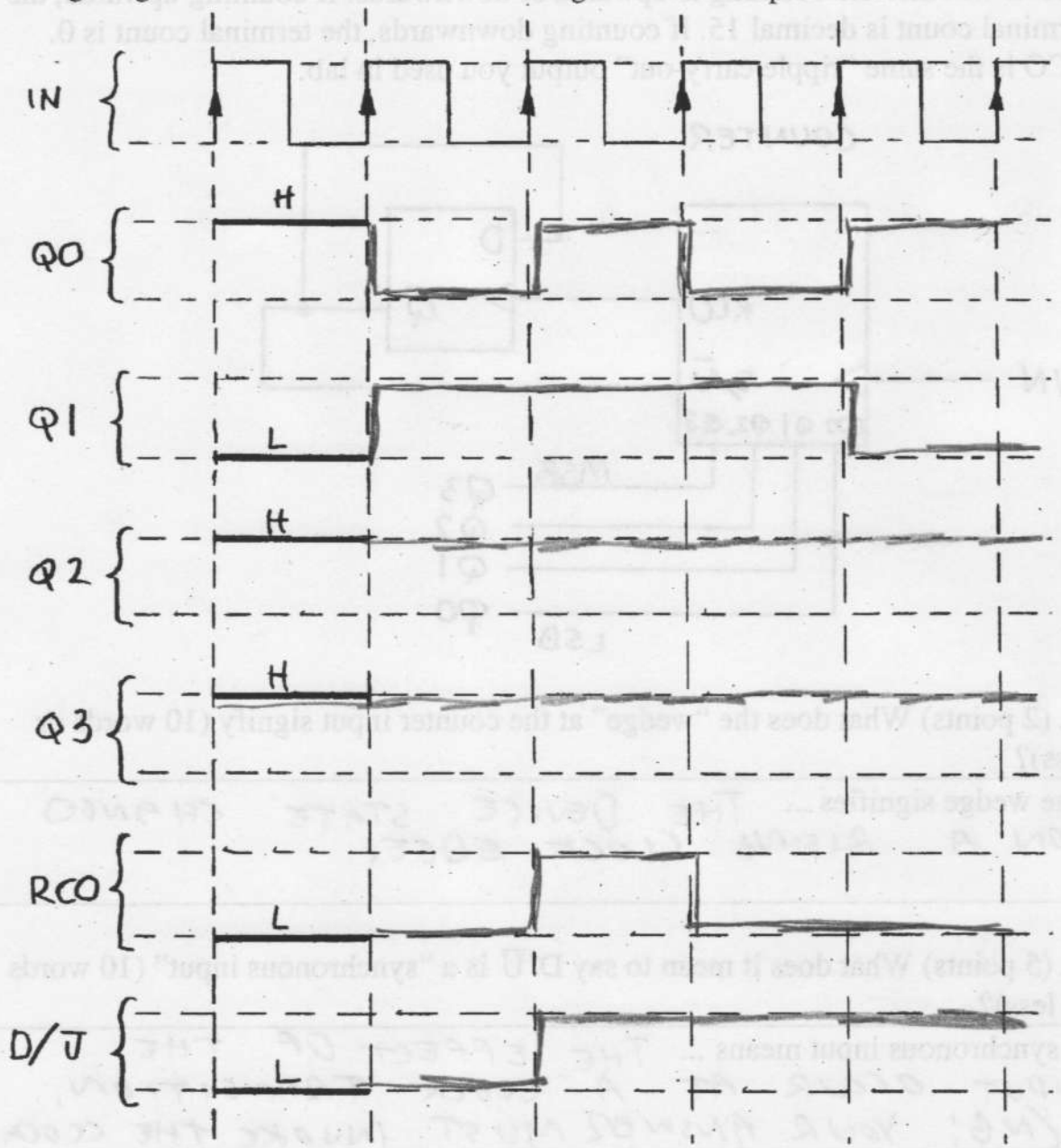
A synchronous input means ... THE EFFECT OF THE INPUT OCCUR AT A CLOCK TRANSITION. (NB! YOUR ANSWER MUST INVOKE THE CLOCK.)

C. (5 points) The D-latch is configured to perform what function (10 words or less)?

The D-latch is configured as a ... DIVIDE-BY-2 COUNTER.

(Problem 3 continued)

D. (10 points) Assume the input "IN" is a square-wave clock. Complete the timing diagram below. Notice the initial logic levels are specified.



E. (4 points) What do "LSB" and "MSB" mean (10 words or less each)?

LSB means ... LEAST SIGNIFICANT BIT.

MSB means ... MOST SIGNIFICANT BIT.

(Problem 3 continued)

F. (4 points) In the timing diagram above, what does the up-arrow on IN signify (10 words or less)?

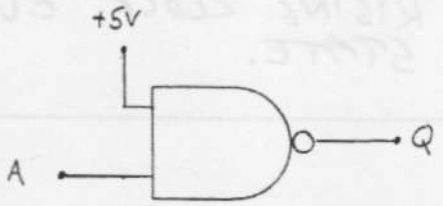
The up-arrow signifies ... THE RISING CLOCK EDGE CHANGES THE DEVICE STATE.

G. (5 points) Suppose the counter outputs are then applied to the input of a 4-bit DAC. (The counter MSB is the DAC MSB, etc.) What is the approximate waveform shape at the DAC output (10 words or less)?

The DAC output waveform looks like a ... AN APPROXIMATION TO A TRIANGLE WAVE

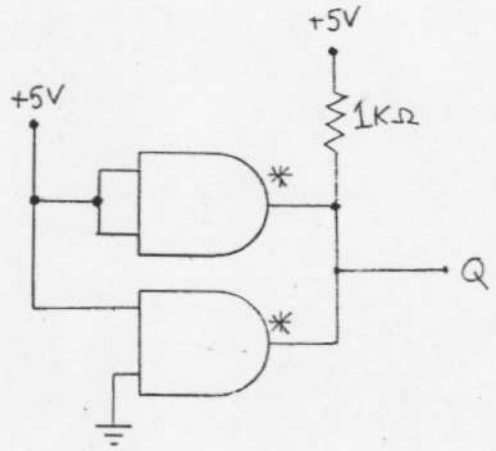
4. (20 points total) Digital circuits: short answers.

A. (4 points) Assume the logic gate below is TTL and input A is floating (left disconnected). What's the value of Q?



Q = LOW (OR "0", OR F). NB. ANSWER OF A GETS PARTIAL CREDIT.

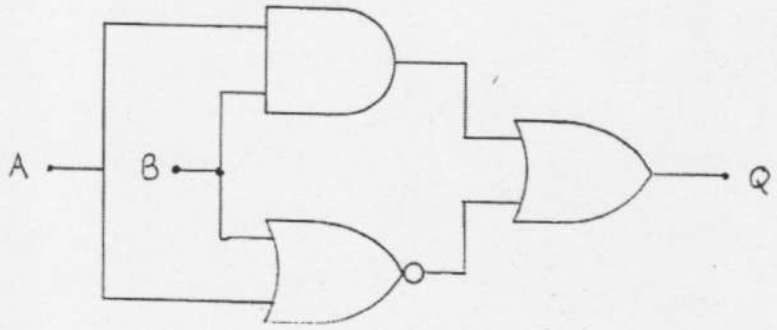
B. (4 points) Two open-collector logic gates are wired as shown. What's the value of Q?



Q = LOW (OR "0", OR "F")

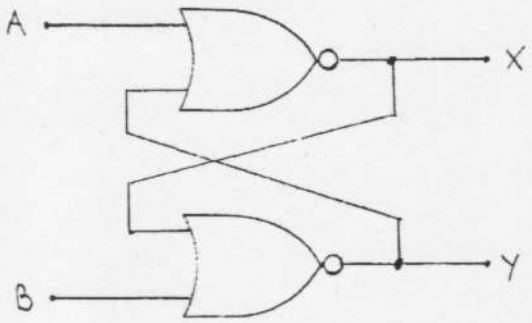
C. (4 points) Fill in the truth table (positive logic)

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	1



D. (4 points) Fill in the truth table, assuming A, B = 1, 1 is followed by 1, 0 then 0, 1 etc. (positive logic)

A	B	X	Y
1	1	0	0
1	0	0	1
0	1	1	0
1	0	0	1



E. (4 points) D-latch: Fill in the timing diagram for Q with CLK and D as shown. Notice that Q starts low. Assume un-shown inputs don't inhibit clocking the chip.