Physics 335, Circuits II
Spring Quarter 2010
Mid-Term Examination

Name SOLUTIONS

1	/30
2	/35
3	/35
TOTAL	/100

Please check that you have a total of 7 pages, including this page.

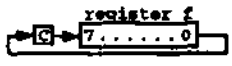
Exam notes: This exam is closed-book. You may use a calculator. There's a summary of PIC instructions on the following page. You can use scratch paper, but the scratch paper won't be graded.

14-Bit Core Instruction Set

14-Bit Core Literal and Control Operations

Hex	Mnemonic		Description	Function
3Ekk	ADDLW	k	Add literal to W	k + W → W
39kk	ANDLW	k	AND literal and W	k .AND. W → W
2kkk	CALL	k	Call subroutine	PC + 1 → TOS, k → PC
0064	CLRWDT	T	Clear watchdog timer	0 → WDT (and Prescaler)
2kkk	GOTO	k	Goto address (k is nine bits)	k → PC(9 bits)
38kk	IORLW	k	Incl. OR literal and W	k .OR. W → W
30kk	MOVLW	k	Move Literal to W	k → W
0062	OPTION		Load OPTION register	W → OPTION Register
0009	RETFIE		Return from interrupt	TOS → PC, 1 → GIE
34kk	RETLW	k	Return with literal in W	k → W, TOS → PC
0008	RETURN		Return from subroutine	TOS → PC
0063	SLEEP		Go into Standby Mode	0 → WDT, stop oscillator
3Ckk	SUBLW	k	Subtract W from literal	k - W → W
006f	TRIS	f	Tristate port f	W → I/O control reg f
3Akk	XORLW	k	Exclusive OR literal and W	k .XOR. W → W

14-Bit Core Byte Oriented File Register Operations

Hex	Mnemonic		Description	Function
07ff	ADDWF	f,d	Add W and f	W + f → d
05ff	ANDWF	f,d	AND W and f	W .AND. f → d
018f	CLRF	f	Clear f	0 → f
0100	CLRW		Clear W	0 → W
09ff	COMF	f,d	Complement f	.NOT. f → d
03ff	DECF	f,d	Decrement f	f - 1 → d
0Bff	DECFSZ	f,d	Decrement f, skip if zero	f - 1 → d, skip if 0
0Aff	INCF	f,d	Increment f	f + 1 → d
0Fff	INCFSZ	f,d	Increment f, skip if zero	f + 1 → d, skip if 0
04ff	IORWF	f,d	Inclusive OR W and f	W .OR. f → d
08ff	MOVF	f,d	Move f	f → d
008f	MOVWF	f	Move W to f	W → f
0000	NOP		No operation	
0Dff	RLF	f,d	Rotate left f	
0Cff	RRF	f,d	Rotate right f	
02ff	SUBWF	f,d	Subtract W from f	f - W → d
0Eff	SWAPF	f,d	Swap halves f	f(0:3) ↔ f(4:7) → d
06ff	XORWF	f,d	Exclusive OR W and f	W .XOR. f → d
1bff	BCF	f,b	Bit clear f	0 → f(b)
1bff	BSF	f,b	Bit set f	1 → f(b)
1bff	BTFSC	f,b	Bit test, skip if clear	skip if f(b) = 0
1bff	BTFSS	f,b	Bit test, skip if set	skip if f(b) = 1

1. (30 points) Simple PIC 16F84A programming.
Find the value of w-register after execution of the following snippets of code. Assume the 16f84a.inc definitions are loaded. Put your answer as a hexadecimal number in the box.

```
movlw H'06'  ;move literal to w
clrw         ;clear w
```

6

w (hex) = 00_{HEX}

```
movlw H'06' ;move literal to w
addlw H'04' ;literal addition to w
```

8

w (hex) = $0A_{HEX}$

```
movlw H'06' ;move literal to w
andlw H'04' ;literal and with w
```

8

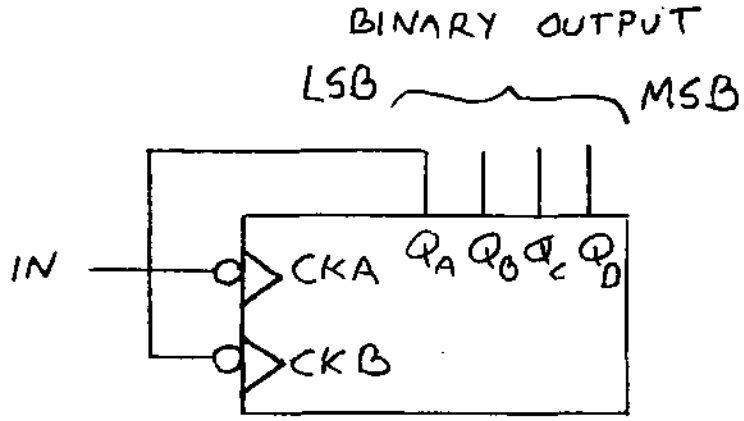
w (hex) = 04_{HEX}

```
movlw H'06' ;move literal to w
movwf H'0E'; move w to location H'0E'
bsf H'0E', D'06' ;bit set
movf H'0E',w ;move
```

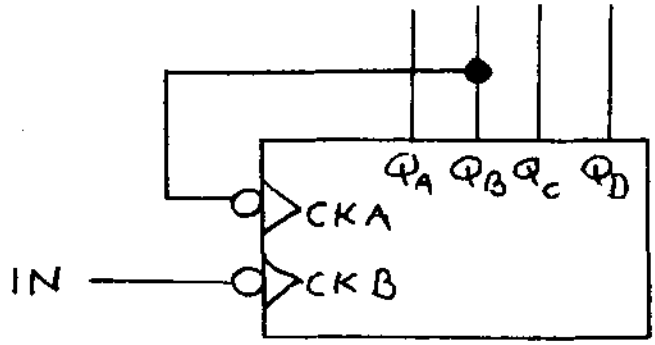
8

w (hex) = 46_{HEX}

2. (35 points) Counters. Recall in lab we used a 74LS93 configured as a 4-bit binary counter. Also recall in lab there was a connection between QA and CKB because this counter has two independent counters, a divide-by-two counter (clocked by CKA with output QA) and a divide-by-eight counter (clocked by CKB with outputs QB, QC and QD).



Now, from this point on, consider the 74LS93 wired as shown below. Assume un-shown inputs don't disable counting.



A. What does the "wedge" at the inputs to CKA and CKB indicate?

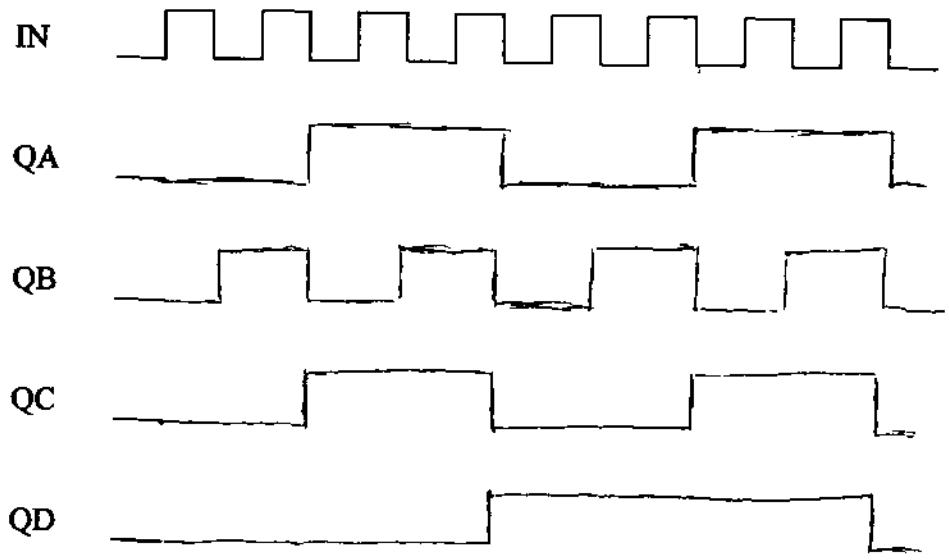
The wedge indicates ... that CKA and CKB trigger on an edge.

B. What does the "open ball" at the inputs to CKA and CKB indicate?

The open ball indicates ... that CKA and CKB trigger on a falling edge.

(problem 2, continued)

C. Complete the timing diagram below. Notice QA through QD start "low".



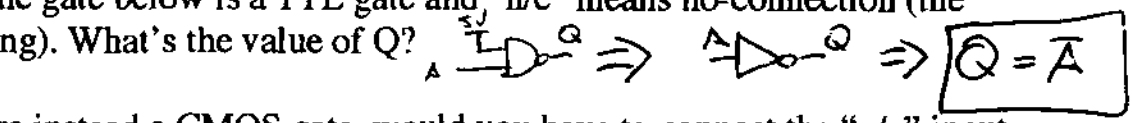
D. Suppose QA, QB, QC and QD are the binary digits in a 4-bit binary number, where QA is the LSB (least-significant bit) and QD the MSD (most-significant bit). What decimal numbers (in the range 0 to 15) will the above counter never output?

It won't output the decimal numbers ...

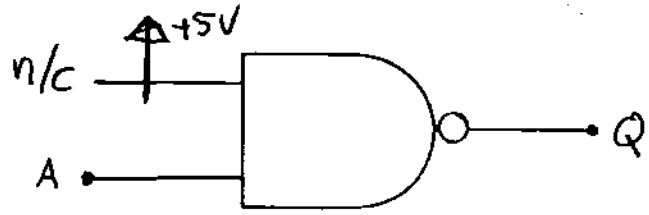
1, 3, 4, 6, 9, 11, 12, 14,

3. (35 points) Digital circuits: short answers. NOTE: TTL INPUTS FLOAT HIGH

A. Assume the gate below is a TTL gate and "n/c" means no-connection (the wire is floating). What's the value of Q?



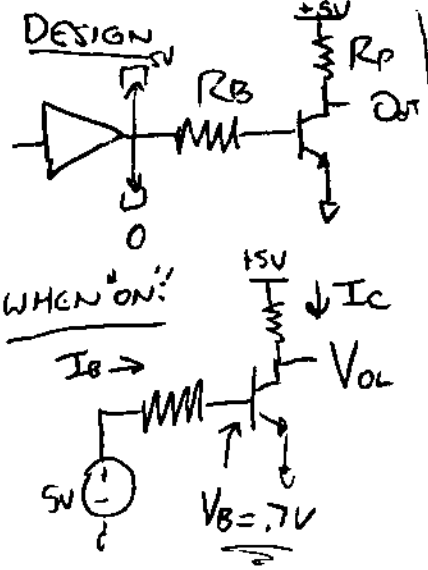
B. If this were instead a CMOS gate, would you have to connect the "n/c" input to ground or +5V or leave it "n/c" to achieve the same functionality as in part A?



IT FLOATS HIGH. IF CMOS, TIE TO +5V.

C. Some circuit contains a non-inverting CMOS "totem-pole"-output logic gate, but you'd like its output to be inverting and open-collector instead. Fortunately, you have a NPN transistor handy. To the left of the figure below, sketch a circuit consisting of the CMOS logic gate, the transistor, plus a single resistor that together mimics an open-collector inverting output. Assume the "beta" of the transistor is approximately 100.

D. Explain how you picked a sensible value for that resistor. Hint: Don't confuse this resistor with a "pull-up" resistor found on open-collector outputs.



STEPS:

① $V_{OH} = 5V$

② V_{OL} = PICK = ~1V

③ PICK REASONABLE I_C, $I_C = 10mA$

④ CALC R_P

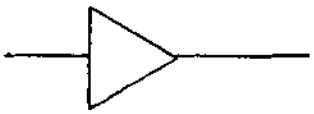
$V_P = (5-1) = I_C R_P$

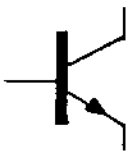
$R_P = 400\Omega$

⑤ WHAT IS I_B?

$I_C = \beta I_B \rightarrow I_B = 100\mu A$

NON-INVERTING GATE





NPN TRANSISTOR

⑥ PICK R_B

$V_B = (5-.7) = I_B R_B$

$R_B = 43k\Omega$

kΩ

E. Fill in the truth table below for this configuration of gates.

$C = D = \overline{A+B} = \bar{A}\bar{B}$

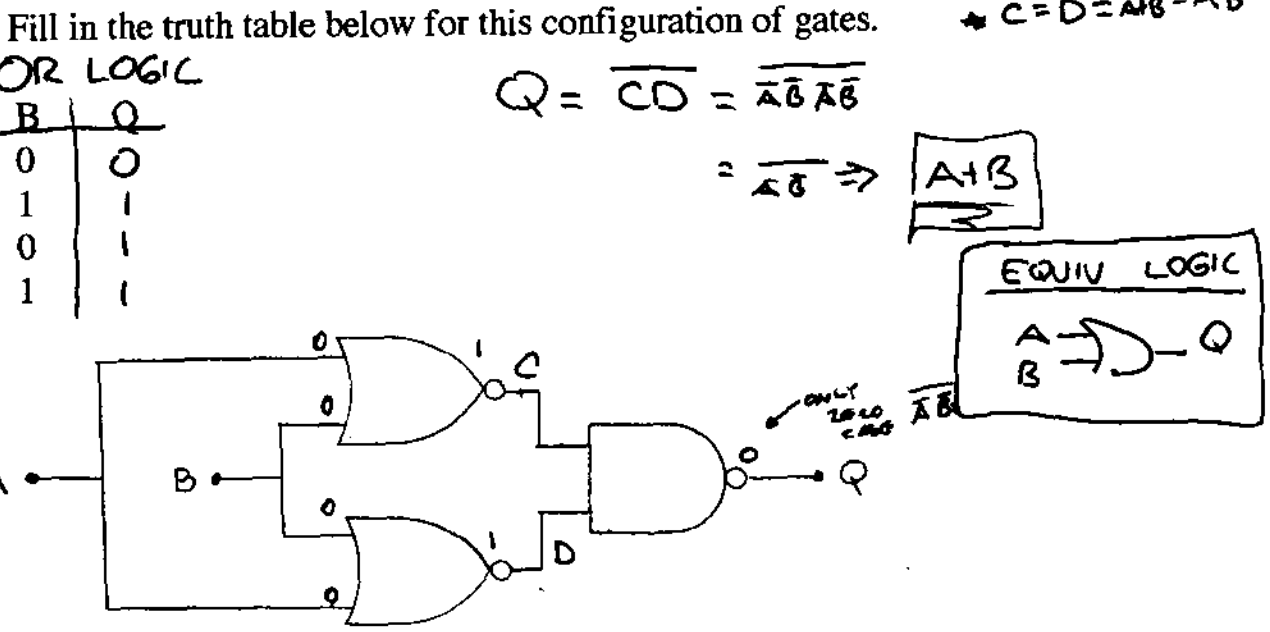
OR LOGIC

A	B	Q
0	0	0
0	1	1
1	0	1
1	1	1

$Q = \overline{CD} = \overline{\bar{A}\bar{B}\,\bar{A}\bar{B}}$

$= \overline{\bar{A}\bar{B}} \Rightarrow A+B$

EQUIV LOGIC



F. For this D-latch, fill in the timing diagram for Q with CLK as shown. Notice that Q starts low. You can assume un-shown inputs don't inhibit clocking the chip.