Either switch position is a ground — real or virtual. Therefore currents don’t depend on switch positions. Notice current entering node C from the left: it divides equally through two 100k resistors. As for node B, the resistance “looking” right is 100k (that is, 50k + 100k/100 = 100k). Hence current entering B splits evenly, the same holds for node A. Hence, at each node, current splits equally.

The current I_0 is \( \frac{10V}{100k \Omega} = 100 \, mA \), hence \( I_1 = 50 \, mA \), \( I_2 = 25 \, mA \), and \( I_3 = I_4 = 12.5 \, mA \).
2) FOR $V_{\text{REF}} = 10\, \text{V}$ with 16 "steps", each step is $10\, \text{V}/16 = 0.625\, \text{V}/\text{count}$.

$7.21\, \text{V}/0.625\, \text{V}/\text{count} \approx 11.5$ counts,

Hence, the 4 MSBs are 1011.

The second ADC sees input $7.21\, \text{V} - 11$ counts $\times 0.625\, \text{V}/\text{count} = 0.335\, \text{V}$.

Notice the "step size" (least count) is $\times 16$ smaller than that of the first ADC: $(10\, \text{V}/16)/16\, \text{V}/\text{count} = 0.039\, \text{V}/\text{count}$.

So, again

$0.335\, \text{V}/0.039\, \text{V}/\text{count} \approx 8.6$ counts.

Hence, the four LSBs are 1000 and the complete 8-bit output is 1011 1000.

(You can quibble about whether to assign count thresholds at the bottom, top, or middle of a step.)