Physics 335  
Homework Set 3  
Due Tuesday, 7 April 2015, 10:30a

Reading


*Before your lab section meets*: Read through Lab 1 - Intro to Digital Logic, available on the course website

Problems

1. Exercise 4.1, p. 92, Galvez.

2. Analyze the TTL gate shown below by answering the following questions.

   ![TTL Gate Diagram]

   (a) Let input voltages be LOW = 0 V and HIGH = +5 V. Make a table that states whether each of the transistors $Q_1$ through $Q_6$ are on or off for all for combinations of HI and LOW on the inputs A and B.

   (b) From this table determine what logic function it represents.

   (c) What current (approximately) flows in an input line when the input is HIGH? What current flows when the input is LOW?

   (d) Without any load, the voltage when the output is HIGH is 3.4 volts. Explain why this is true.

   (e) If, when the output was HIGH, the output current was 1.5 mA, what would the output voltage be? Explain and/or show a calculation that supports your answer.
3. Analyze the CMOS gate shown below. Determine what logic function it represents.